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Implementation of High Speed FFT using Reversible Logic Gates for Wireless DSP Applications

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Abstract

The proposed FFT is constructed using Modified Reversible Logic Gates logic using Ripple carry Adder and its performance is compared with the existing Multiplier Circuits. This type of adders can be applied in the field of digital image processing and signal processing where importance is given to accuracy. The design will be implemented and simulated using Xilinx-ISE-Simulator and performance will be tested. The proposed Reversible Logic Gates logic implemented in Ripple carry adder system using xor logic has an accuracy of 99.98% and power consumption has reduced by more than 75%. Implementation of Modified Reversible Logic Gates logic using xor logic is done using the Xilinx-ISE-simulator tool. Using this adder we have designed an Multiplier based on the Vedic mathematics computation using reversible logic gates. The Vedic multiplier is implemented in FFT, which uses Urdhva Tiryabhyam, Nikhilam Navatashcaramam Dashatah, and Anurupye Vedic mathematical algorithms. The N point DFT is computed by using efficient Fast Fourier transform (FFT) algorithm. It's necessary for a multiplier to be fast and power efficient in order to make this process rapid and simple. It is used to solve partial differential equations and also to perform convolution operations.

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Keywords: Type your keywords here, separated by semicolons ;

1. Introduction

The core intention of this proposed modified Ripple carry adder is to propose a low power high speed VLSI "adder subsystem" to increase the CPU performance and the entire Design of the Ripple carry adder is implemented with Backend tools. The performance improvement of a CPU is directly dependent on the performance of the subsystems. The adder subsystem is the heart of a processor, with its manipulation, other than addition, operations like subtraction, multiplication and address fetching can be achieved. Hence, this proposed Modified Reversible Logic Gates logic based RCA, Adder made a novel technique which reduces the power, delay, and no of transistors when compared to the previous logic. In previous paper [1] work we have already implemented a 4 * 4 Vedic multiplier using reversible logic. In that multiplier we have implemented by using ripple carry adder using reversible logic gates. In this paper we have modified our xor logic by using Modified Reversible Logic Gate design. By using proposed logic we have designed a ripple carry adder which executes high speed carry addition operation simulated by using the Backend tool called Cadence. The output of the Modified Reversible Logic Gates logic based Ripple carry adder is compared with existing adder like Carry select adder, carry shift logic, and carry look ahead adder. The proposed Modified Reversible Logic Gates logic XOR logic based Ripple carry adder has reduced the delay, power, size and no of transistor count when compared to the previous logic.

DFT can be applied to numerous tasks, including FFT, and likewise, also to image enhancement. In order to improve things, we must find the solution. Fast execution of the FFT and DFT

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operations should be expected. The Vedic multipliers use less power and work compared to traditional ones such multipliers such as Wallace, but are faster to complete. Speed and performance also depend on the number of additions and multiplications that take place in the system at any given time. Because of the use of parallel adders, the long multiplication will increase. (To make a mixture). Partial Products Generation (PPG), PPG and Partial Products Addition (PPA) both expand in the first two steps and end users to increase the total product in the third Final Convectional Addition (FCA). When it comes to the main concerns, the biggest issue is that the multipliers move more slowly.

2. Proposed Method :-

Our proposed modified reversible logic gates based RCA Adder will overcome all the drawbacks faced in the existing Our proposed modified reversible logic gates based RCA Adder has finds a solution to address all of the issues & drawbacks faced in the existing Ripple Carry adder(RCA) systems. The output comparison can be done by using the simulator software called Xilinx-ISE-10.1 and The graph above shows that the proposed modifiable reversible logic gates based RCA Adder has reduced the delay, power, area, and not of transistor count compared to the existing adder techniques. Our previous work, which used modified reversible logic functions, is depicted in the diagram above. Adder shows how to calculate 4x high speed in a simple way. Internet access with high-speed A Modified RCA multiplier is created by swapping out two classic RCA multipliers for two improved versions. The 4x4 High Speed Multiplier's top-level diagram is depicted in this diagram. Each block has four times two bits of input and four bits of output, as illustrated in the block diagram

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3. Vedic Mathematics :-

The sixteen sutra of Vedic maths are listed below. The thirteen upa sutras are also listed below. The main issue is to increase the speed of the multiplier partial products should be reduced. The product of the sum is the sum of the products of the Vedic mathematician's previous foundations

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The thirteen upa- sutras of Vedic mathematics are listed below.

S.n.o	Name of The Sutras	Description
1.	Anurupyena	Proportionality
2.	Sisyate Sesasmjnah	The remainder remains constant
3.	Adyamadyenantyamantyena	The first by the first and the last by the last
4.	Kevalaih Saptakam Gunyat	For 7 the multiplicand is 143
5.	Vestanam	By osculation
6.	Yavadunam Tavadunam	Lesser by the deficiency
7.	Yavadunam Tavadunikrtya Vargnca Yojayet	Whatever the deficiency lesser by the amount and set up the square of the deficiency
8.	Antyayordasake'pi	Last totalling 10
9.	Antyayoreva	Only the last terms
10.	Samuccayagunitah	The sum of the product
11.	Lopanasthapanabhyam	By alternate elimination and retention
12.	Vilokanam	My mere observation
13.	Gunitasmuccayah Samuccayagunitah	The product of the sum is the sum of the products
15.	Vyashtisamanstih	Part and whole
16.	Yaavadunam	Whatever the extent of its deficiency

4. Reversible logic:

Reversible logic has its basics from thermodynamics of information processing. According to this, traditional irreversible circuits generate heat due to the loss of information during computation.. A circuit that is built from reversible gates is known as a reversible logic circuit. Some of the reversible gates are shown below that are used in the proposed design. The representation of a 3*3 reversible gate is shown below. The Quantum cost of this gate is 4.4 joules. The circuit should contain at least the minimum number of reversible gates as possible to achieve reversibility. It is calculated knowing the number of primitive reversible gates (1*1 or 2*2) required to realize the circuit. The design parameters are below: Garbage outputs (GO), Gate Counts (GC), Constant inputs (CI) and Quantum cost (QC) The circuit is said to be reversible when it contains at least four reversible gates.

5.1 Toffile Gate

Toffile gate is a 3*3 reversible gate. Peres gate is one of the popular gate and used in many applications. BME gate has four inputs and four outputs. The quantum cost of this gate is 6.2 * 6. Toffile and BME gates are reversible. While designing the circuit using reversible logic gates the designer should concentrate on the following parameters

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S.N.O	PARAMETERS OF REVERSIBLE LOGIC GATES	DESCRIPTION
1.	. Garbage Outputs(GO)	Indicates the unused outputs in the circuit which cannot be avoided and it is necessary to achieve reversibility. The circuit should contain minimum number of garbage outputs
2.	Constant inputs (CI)	This refers to the number of inputs that are to be maintained constant at either 0 or 1 in order to synthesize the given logical function
3.	Gate Counts (GC)	Indicates the number of reversible gates that are required to design the circuit, so that the circuit should contain reversible gates as minimum as possible
4.	Quantum cost (QC)	This refers to the cost of the circuit in terms of the cost of a primitive gate. It is calculated knowing the number of primitive reversible logic gates (1*1 or 2*2) required to realize the circuit

Some of the reversible logic gates are shown below that are used in the proposed design:

5.2 PERES GATE: It is a 3*3 reversible gate i.e., it has three inputs and three outputs. The representation of Peres gate is shown below. Quantum cost of this gate is 4.

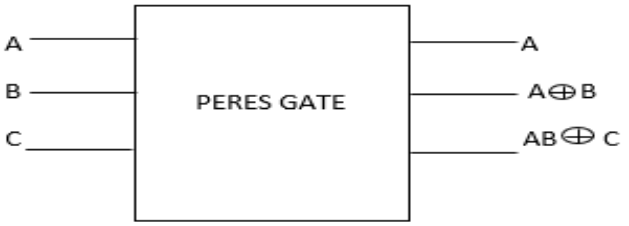

Fig.1: Peres gate.

Peres gate is one of the popular gate and used in many applications.

5.3 TOFFOLI GATE: It is a 3*3 reversible gate i.e., it has three inputs and three outputs. The representation of Toffile gate is shown below. Quantum cost of this gate is 5.

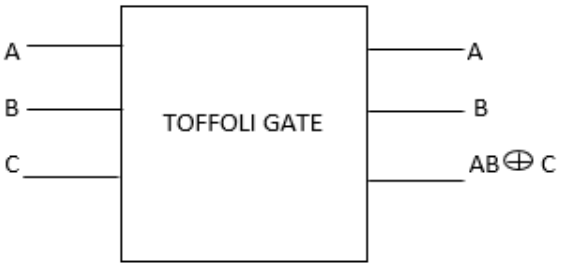

Fig.2: Toffoli gate.

5.4 BME GATE:

It is a 4*4 reversible gate i.e., it has four inputs and four outputs. The representation of BME gate is shown below. The quantum cost of this gate is 6.

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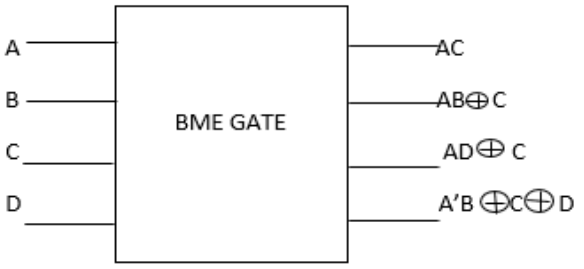

Fig.3: BME gate.

5.5 Structure of Urdhva 2x2 Vedic Multiplier

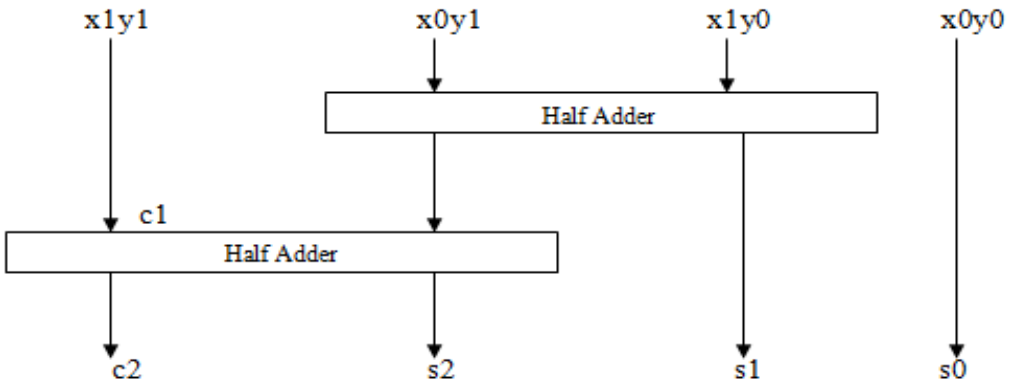

Figure 4.Structure of Urdhva 2x2 Vedic Multiplier

The Urdhva tiryakbhyam Sutra is applied to the binary number system to create a digital multiplier architecture. This is similar to the widely used array multiplier design. As shown in Fig 4, the method is described for two 2-bit numbers X and Y, where X = x1x0 and B = y1y0. Booth multiplication is another important multiplication algorithm. Large booth arrays are required for high-speed applications, and it allows for a quick multiplication of two numbers. Because it requires a large number of no gates, an array multiplier is more expensive.

The algorithm is depicted in the figure below. 101 times 110 is a multiple of 101.

1. First, take the right-hand digits from both the multiplicand and the multiplier. Then add them all together. Then we'll get the answer's LSB digit.
2. Multiply the top number's second bit by the bottom number's LSB. Then multiply the top number's LSB by the bottom number's second bit. Then add them up to get the second part of the answer.
3. Multiply the third bit of the bottom number by the LSB of the top number, the second bit of the bottom number by the second bit of the top number, and the third bit of the top number by the LSB of the bottom number. Then add them to get the third part of the answer.

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4. Repeat the second step, but this time moves one space to the left. We'll multiply one number's second digit by the other number's MSB.
5. Finally, to get the final product, multiply the LSB of the top and bottom numbers.

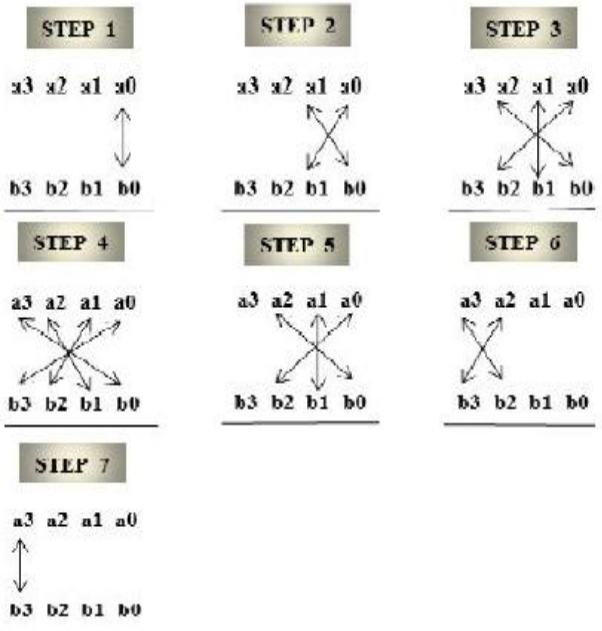

Fig.5: MULTIPLICATION OF TWO 4 BIT NUMBERS USING URDHVA TIRYAKBHYAM.

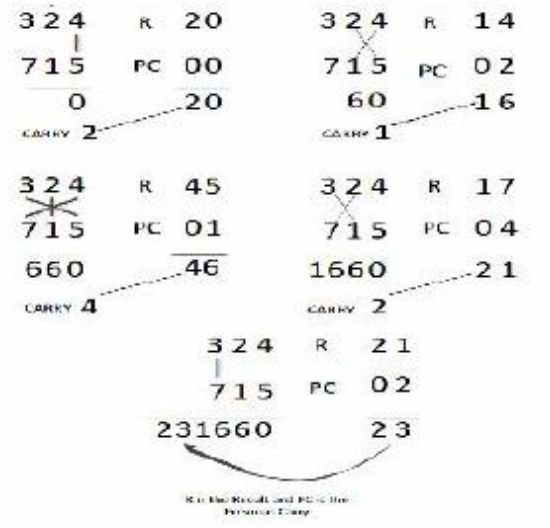

Fig.6: URDHVA TIRYAKBHYAM ALGORITHM FOR DECIMAL MULTIPLICATION.

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5. Proposed System:-

The existing adder system designs are the conventional adder designs that usually consist of a long carry propagation chain for serial addition. Such adders so far exists are the Ripple Carry Adder, Carry Look-Ahead adder and few high speed adders using Pass-transistor logic and Transmission gate logic will increases the power, Delay ,size and no of transistor counts. Our proposed ripple carry adder using Modified reversible logic will overcome all the drawbacks faced in the existing system. The output comparison can be done by using the Simulator Software tool called Xilinx-ISE-simulator. and it shows that the proposed Modified reversible logic Ripple carry adder has reduced the delay,power,area,and not of transistor count compared to the existing adder techniques. The figure 7 shows our previous research work based on 4 * 4 Vedic multiplier by using reversible logic gates. Now in future we are going to modify the Existing ripple carry adder with our proposed logic. Which in further reduces the size, area, and power.

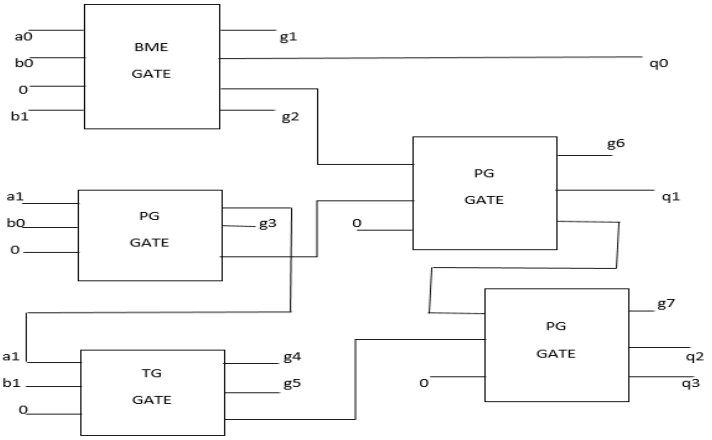

Fig 7a proposed 2*2 Vedic multiplier using Reversible logic gates

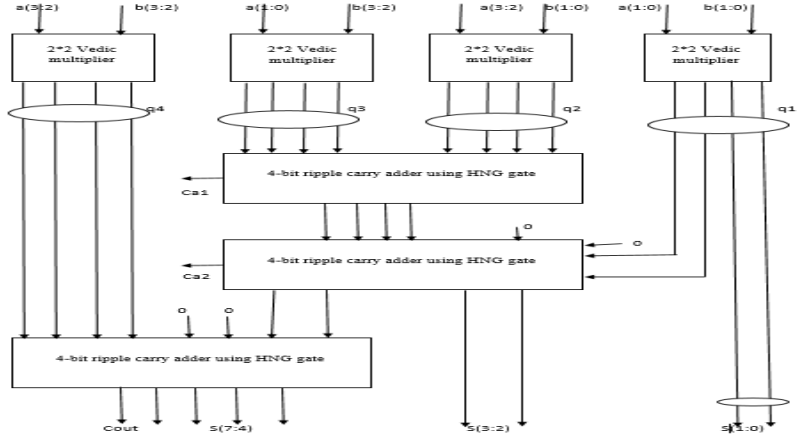

Fig. 7b . Block diagram of Reversible 4*4 Vedic multiplier

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Designing a low-power VLSI sub system has turn into a significant performance objective because of the high-speed budding technology in mobile computation and communication. Most of the works concentrated basically on reducing the size and number of transistor used in the design. We have designed Modified reversible loic gate and hence managed to bring down the transistor count which is nothing but the drop in area, power utilization and delay in the circuit. The importance given to the design of reversible logic gate is because of the fact that most of the systems constitute HNO gate circuits associated with other circuits. As in case of a HNO based Ripple carry adder, random number generator etc., reversible logic gates plays a major part. Hence the improvement in performance of an adder subsystem and so on. the schematic diagram of ripple carry adder is shown in fig6. For better observation of the output results, the gates can be connected to an adder and the performance of each can be compared with existing technique.

5.1. Drawbacks In The Existing System

Power is one of the peak factor resources of the designer tries to save when designing a VLSI based sub system. The goal is to increase the battery life time of portable electronic devices, by reducing the no of transistors, power consumption and to decrease the power spent per arithmetic operation, however lower power utilization does not essentially bring about lower energy dissipation and higher performance. To execute mathematics operations, a device can use very low power by functioning at very low frequency but it may use extremely a long time to finish the operation. For that reason we calculate the energy indulgence and evaluate the performance of the system by calculating the Power Delay Product (PDP), which is the product of normal power consumption and worst case delay. All these are the important factors of performance evaluation for any VLSI subsystem. When these are taken into consideration, then the conventional adders fails to achieve certain requirements. Here is always a exchange between power consumption and speed of the processing unit. Also there is a cost spent for the sizes of the system with newer logics bringing in more transistors. These were the major drawbacks of the existing system.

6. Proposed High speed FFT Transform using modified reversible logic gates

The performance of high speed multiplier is to be improved which is designed based on different Vedic sutras can be implemented by using modified high reversible logic based carry select adder Urdhva tiryabhyam, Nikhilam Navatashcaramam Dashatah, Anurupye Vedic mathematical algorithm. By using this multiplier, computation time for NxN bits is to be reduced. Fast Fourier transforms (FFT) transforms of a DSP processor is to be implemented by these NxN multiplier and compare the following factors in the above three sutras: The calculation time for the multiplication of bits is to be minimized. The worst case propagation delay in the optimized Vedic multiplier case is 32.16ns. The Vedic multiplier is implemented in FFT, which uses Urdhva Tiryabhyam, Nikhilam Navatashcaramam Dashatah, and Anurupye Vedic mathematical algorithms. The N point DFT is computed by using efficient Fast Fourier transform (FFT) algorithm. It's essential for the multiplier to be high-speed and power efficient in order to make this process rapid and simple. It is used to solve partial differential equations and also to perform convolution operations

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7. Implementation of Vedic Sutras in Fast Fourier transforms using Modified reversible logic

Vedic algorithm is proposed for the implementation of multipliers that are used significantly in Fast Fourier Transform (FFT) and it provides fast and reliable approach to compute the N point DFT**.** Eq. 1. Shows the DFT function of X (k) that is an *N*-point sequence of x (n).

$$X(k) = \sum_{n=0}^{N=1} x(n) \exp^{\left\{-j\left(\frac{2\Pi}{N}\right)kn\right\}}, 0 \le k \le N-1 \quad (1)$$

The simplified notation of DFT is mentioned in Eq. 2,

$$X(k) = \sum_{n=0}^{N-1} x(n) W_N^{kn}, 0 \le k \le N-1 \quad (2)$$

8. Results & Comparison of various Vedic FFT Mathematic computation sutras

The Output window for 8x8 Anurupye Vedic Multiplier which was implemented in FFT is shown in Fig.8. It performs multiplication of two decimal numbers 58 x 48 by "If one is in ratio, the other is zero operation" (Anurupye method). Using the Output window for 8x8 Urdhva Vedic Multiplier which was implemented in FFT is shown in Fig.9 It performs multiplication of two decimal numbers 154 x 142 by "Vertical and crosswise multiplications" (Urdhva- Tiryakbhyam method). The Output window for 8x8 Nikhilam Vedic Multiplier which was implemented in FFT is shown in Fig.10. It performs multiplication of two decimal numbers 97 x 94 by "all from 9 and last from 10 operations" (Nikhilam method). The performance analysis of Vedic multiplier using modified reversible logic with high speed and low delay performance characteristics are represented in the Table

9. RESULTS AND DISCUSSIONS

The Output window for 8x8 Anurupye Vedic Multiplier which was implemented in FFT is shown in Fig.8.

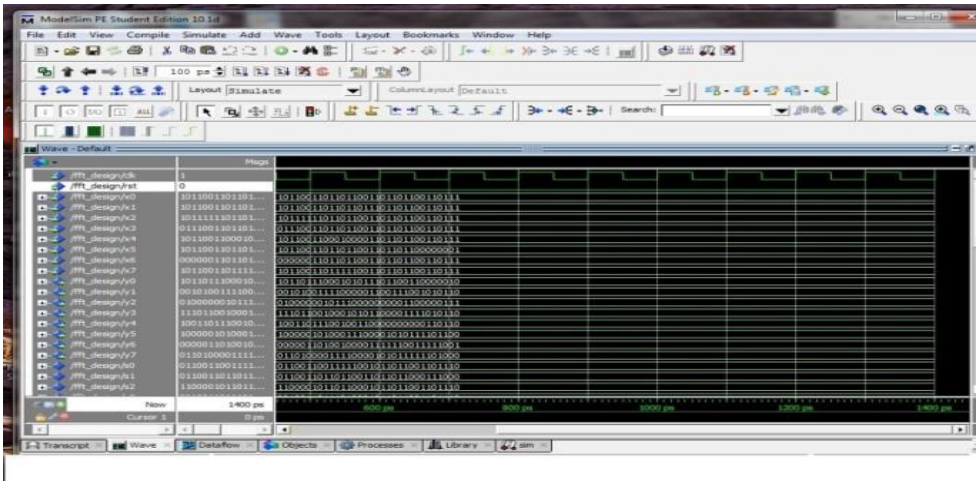

Figure 8.Simulation Output window for 8x8 Anurupye Vedic Multiplier using Modified reversible logic which implemented in FFT

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The Output window for 8x8 Urdhva Vedic Multiplier which was implemented in FFT is shown in Fig.9. It performs multiplication of two decimal numbers 154 x 142 by "Vertical and crosswise multiplications" (Urdhva- Tiryakbhyam method).

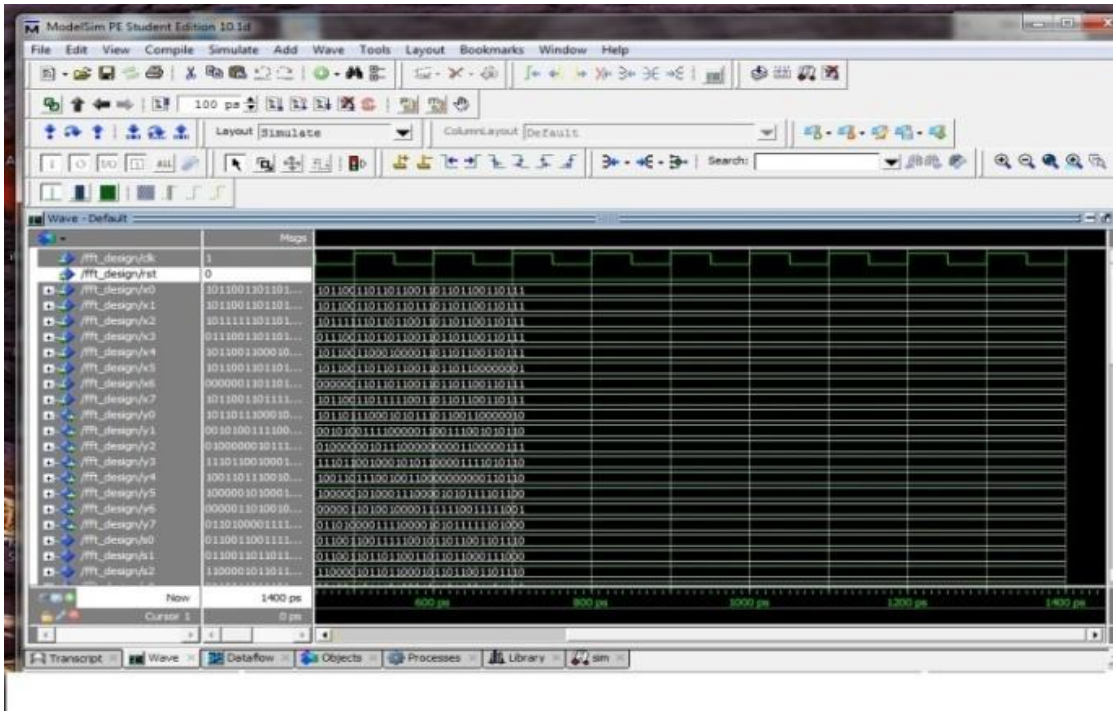

Figure 9.Simulation Output window for 8x8 Urdhva Vedic Multiplier which implemented in FFT

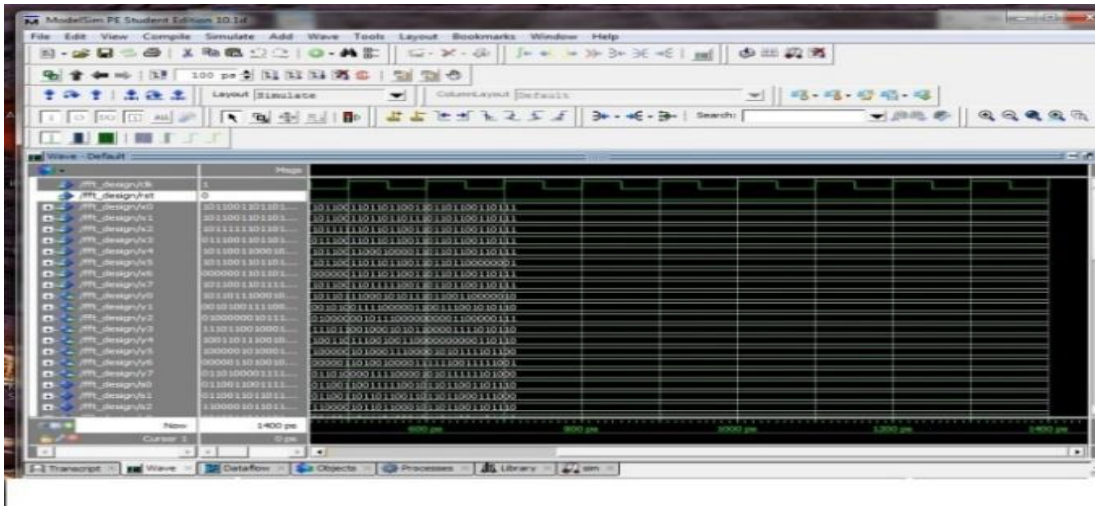

Fig.10. Simulation Output window for Nikhilam Vedic Multiplier which implemented in FFT

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Figure 11. delay calculatation for the proposed 8 * 8 FFT by using **Anurupye Vedic Multiplier using Modified reversible logic**

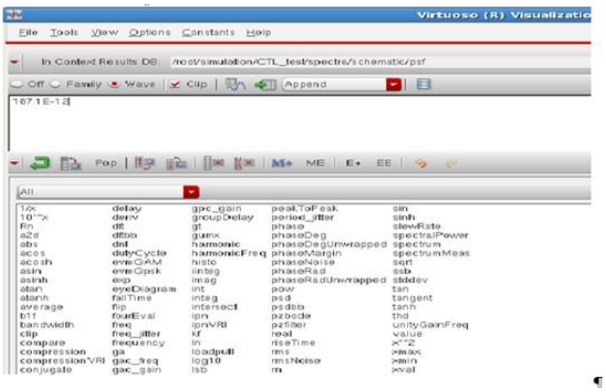

Fig12. Delay calculation for the Existing Simulation Output window for 8x8 Urdhva Vedic Multiplier

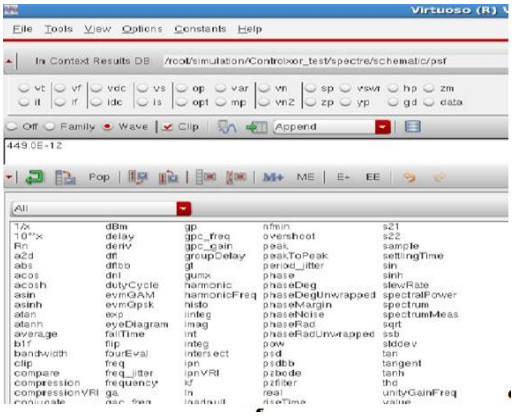

Table 4. Comparison of Various Adders with our Proposed reversible logic gate based RCA.

Type of Adder	Power (mW)	Delay (ns)	PDP (pJ)	Transistor count
Existing Ripple Carry Adder (E-RCA)	0.22	4.49	0.89	902
Proposed Ripple Carry Adder (P-RCA)	0.13	1.87	0.28	856
Carry Lookahead Adder (CLA)	5.1	2.37	1.21	2208
Carry Shift Adder(CSL)	6	3.06	1.81	2176

Table 5. Performance characteristics.

Modified reversible logic based FFT	Time constraint(delay)
8x8 multiplier using Nikhilam sutra	26.196 ns
8x8 multiplier using Urdhva sutra	18.844 ns
8x8 multiplier using Anurupye sutra	14 ns

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The above is the screen shots of the Delay calculation for the 8 bit reversible logic gate based RCA. The above calculation is done after analysis after Modified reversible logic gate based RCA output. The screenshots show the Output response for the 8 bit reversible logic based RCA adder.

10. Conclusions

The concept of Modifed reversible logic gate is introduced in VLSI design. The Modified reversible logic based Ripple carry adder" which trades certain amount of accuracy for significant power saving and high speed operation. The Proposed reversible logic based RCA adder is simulated using Xilinx –ISE-Simulator tool. The proposed Adder which Extensive comparisons with conventional digital adders showed that the proposed reversible logic based RCA output performance shows that it reduces the overall power consumption, power delay product ,no of transistor count and increases the speed which in turn performs high speed arithmetic operations. By using this vedic sutras technique we have implemented a 8*8 vedic multiplier using ANURUPYE sutras and by using this multiplier we have implemented in Fast fourier transform and it has performs a high speed computation process when compared to other sutras using reversible logic gates.

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