Annals of R.S.C.B., ISSN:1583-6258, Vol. 25, Issue 6, 2021, Pages. 2947 - 2957
Received 25 April 2021; Accepted 08 May 2021.

A Fault Tolerant Pipelined Double Precision Reversible Floating Point Adder/Subtract or in FPGA

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Abstract:Inrealworldcomputation,therearetwomethodologies by which numbers can be stored they arefixed point notation and floating point notation. Floatingpoint operations are used to a greater extent in most of thecomputationaldevices.FrequentlyusedoperationisFloating point addition and Subtraction. In Applicationssuch as, Digital Signal Processing and Optical computingSpeed of operation and low power consumptions are themajor criteria. Reversible logic provides a solution for thisproblem.InthispaperaDoubleprecisionPipelinedReversiblefloatingpointadder/subtractor(RFPA)isdesignedusingKMDgates.TheRFPAhasReversibleConditionalswapping,Reversibleadder,ReversibleNormalization and Reversible round off blocks in it. TheDesigned RFPA is coded using Verilog and the same hasbeen simulated using Modelsim 10.7c. Parameters such asMaximum operation frequencyand logiccellutilizationarecalculatedusingQuartusPrimeedition20.2using10CX220YF672I5G device with respect to Cyclone 10 GXfamily.TheresultshasbeencomparedbetweenSingleprecision and Double precision RFPA which shows thatDouble precision RFPA has greater operating speed by afactorof1.1 attheexpenseofhigherlogiccellutilization.

Keywords:Reversiblelogic,RFPA,Maximumoperatingfrequency.

I. INTRODUCTION

The roadmap for the semiconductors has predicted beyond thenanotechnology it is highly impossible to shrink the devices.Even if the devices are shrunk it may lead to second ordereffects.Anewtechnologymustbeevolvedtokeepthemoore'slawalive.[1,2].Landauerprovedthat,anyirreversible or conventional computation will dissipate KTln2Joules (k is Boltzmann's constant and T is the temperature) ofheatsinceitlosesbitinformationfromin-puttooutputtransition[3].Reversiblelogicisbasedononetoonemapping. A reversible logic circuit has an equal number ofinputs and outputs. The input of a reversible circuit can beuniquely identified from its output.[4]. Reversible logic canbe used to prevent the loss of information during operationsandalsousedintheemergingtechnologieslikeQuantumComputing,QuantumDotCellular AutomataandDigital

Signal Processing [5]. This fault tolerant /detection approachcan beaccomplishedby parity-preservinggates,whereretheinputparityisequal to the outputparity[6].

The arithmetic operation that is performed in most of the DSPprocessorsmakesuseoffloatingpointoperations.Mostwidely used representation of

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floating point numbers is IEEE754standardrepresentation.Thisrepresentedareoftwotypes.

1. SinglePrecisionRepresentation
2. DoublePrecisionRepresentation.

Figure1and2showstherepresentationofboththeformats.

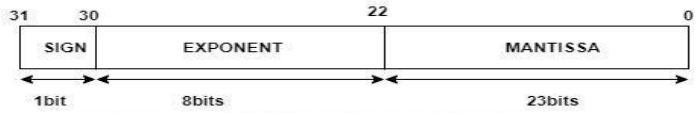

Fig.1.IEEE754singleprecisionfloatingpoint Dataformat

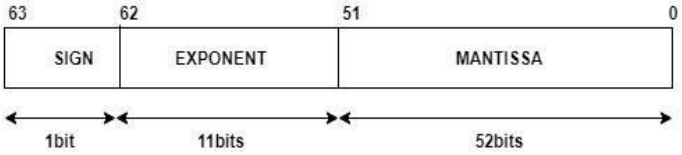

Fig.2.IEEE754DoubleprecisionfloatingpointDataformat

In single precision, there are 32 bits, the MSB bit is sign bit,8 bits are exponent and the last 23 bits are mantissaIn doubleprecision,there are 64bits,the MSBbit is sign bit, next11bits are exponent and the last 52 bits aremantissa. The bitrange of floating point values aredescribed in Table-I. Thebiasvaluefor DoublePrecisionFloatingPointis1023.

TABLE I. BITRANGEOFFLOATINGPOINTVALUES

Precision	SignBit	Exponent	Mantissa
Single	1(31)	8 (30-23)	23(22-00)
Double	1(63)	11(62-52)	52 (51-00)

The paper is structured as follows; Section II reviews a fewreversible logic primitives. Section III explains the reversiblegateusedinthisproposedarchitecture.SectionIVbrieflyoutlines the floating point adder architecture and gives detailsabout its major reversible components. Section V discusses theresultsandSectionVIconcludesthepaperfollowedbyreferences.

II. REVERSIBLELOGICPRIMITIVES

The logic gates that are generally used (AND, OR, NAND,NOR, XOR and XNOR) are irreversible [3].Reversible gatessuch as Feynman, Toffoli, Peres, Fredkin, HNG and TSG aredeveloped by the researchers.These gates are defined by theirnumber ofinputsandoutputs.

A. Quantumcost:

The number of 1×1 and 2×2 reversible gates or quantumgates required in the architecture is known as the quantum costof the reversible gate . The quantum costs of all reversible 1×1and 2×2gatesaretakenasunity[7].

B. Garbageoutputs:

The unusedoutputs foundin reversible circuits are knownasgarbage outputs[6].

C. LogicalCalculations:

LogicalcalculationsreferthetotalnumberofXOR(α),AND(β)andNOT(γ)operationsrequiredtoreal izethefunction[8].

D. Reversibility:

The function f (x_1, x_2 … x_n) of n Boolean variables

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iscalledreversibleifthenumberofoutputsisequaltothenumberofinputsandanyinputpatternmapstoauniqueoutputpattern [9, 10].

E. Universality:

Areversiblegateissaidtobesatisfyinguniversalityproperty only when it could be able to realize NOT, NAND /AND&NOR/ORfunctions[11].

F. Fault-tolerance:

Fault-toleranceisamethodtopreservesameparitybetween input and output vectors over one to one mapping ofthe reversible circuit [12-14]. The input and output vectors of anyfault-tolerantgatesare$I_v\{I_{n-1},I_{n-2},\ldots I_0\}andO_v\{O_{n-1},O_{n-2},\ldots O_0\}$wherethe followingmustbepreserved

$$I_{n-1}\oplus I_{n-2}\oplus\ldots\oplus I_0=O_{n-1}\oplus O_{n-2}\oplus\ldots O_0$$

III. PROPOSEDREVERSIBLEGATE

A.KMDGate 4:

The reversible gates used in this paper are KMD gate. KMDis a 5×5 parity preserving reversible gate.This gateisalsoknownasonethroughbecauseoneofitsinput is also anoutput.Figure3showsthegeneralstructureofKMDgate4.

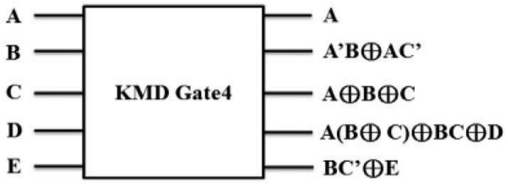

Fig.3KMDGate 4

A single KMD Gate 4 can be used as a full adder. Out oftheavailable5inputs,4inputshavetobeusedtomakea KMDgatetoworkasa1bitfulladder.ThestructureoftheKMDgate asafulladder isshowninthefigure4.

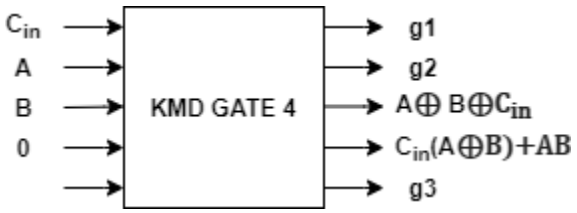

Fig.4KMDgateasaFull Adder

IV. FLOATINGPOINTADDER/SUBTRACTOR

The procedure for adding/ subtracting two floating pointnumbersinIEEE754DoubleprecisionformatconsistofThree major steps.Figure 5 shows the Pipelined ArchitectureofRFPA.

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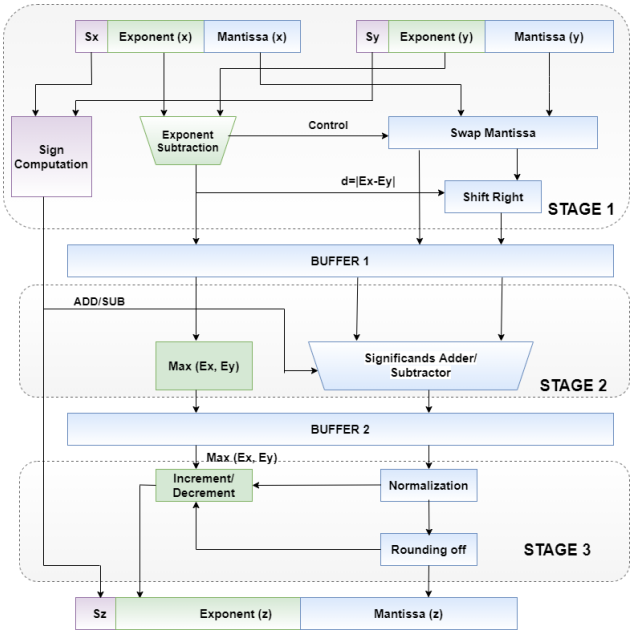

Fig.5PipelinedReversiblefloatingpoint Adder/Subtractor(RFPA)

Two Double precision floating point numbers are fed as theinput in IEEE 754 standard. Each number contains a Sign bit,11 bit Exponent and a 52 bit Mantissa. There are 3 stages ofcompution, in which a buffer is added at the end of each stagetosupportpipelining.Inthefirststagetwoexponentsaresubtracted to check which among them is smaller. The smallerexponent is incremented unitl it aligns with the larger. Uponincrementing the exponent , the mantissa of smaller exponentis shifted right toalignwith thesmaller exponentwithoutaltering its value.In thesecondstagetheSignificands areadded using Reversible KMD adder. In the third stage the sumisnormalizedandroundedofftogetthedesiredvalue.Figure5 illustrates the Pipelined Architecture of Reversible floatingpointadder/subtrator.

A. Reversible Compareand Shiftunit

The first stage of the Architecture is Compare and Shiftoperation.Theexponentsofthetwofloatingpointnumbersaresubtracted.Theminuendistwo' scomplementedandthedifferenceiscalculated.InthisPaper,an11bit2'scomplementReversibleE xponentSubtractorisproposedbasedonKMDgate4.TheMSBbitoftheExponentsubtractor acts as the control input to the swap mantissa block.If Exponent(X) > Exponent (Y) the positions of their mantissaare retained as it is, if not the positions are swapped beforepassing the same to next stage. Once they are swapped, forthe rest of the computation process it is assumed that floatingpoint number X has greater exponent compared to Y.Themagnitude of the Exponent subtractor contains the amount bywhichtheMantissaofthesmallerexponentmustbeshifted.

Once the difference is extracted it is presented as the inputto Shift Right block in which the Mantissa (Y) is shifted bydesiredvalue.TheFigure6Show theRTL schematicofCompareandShiftblock.

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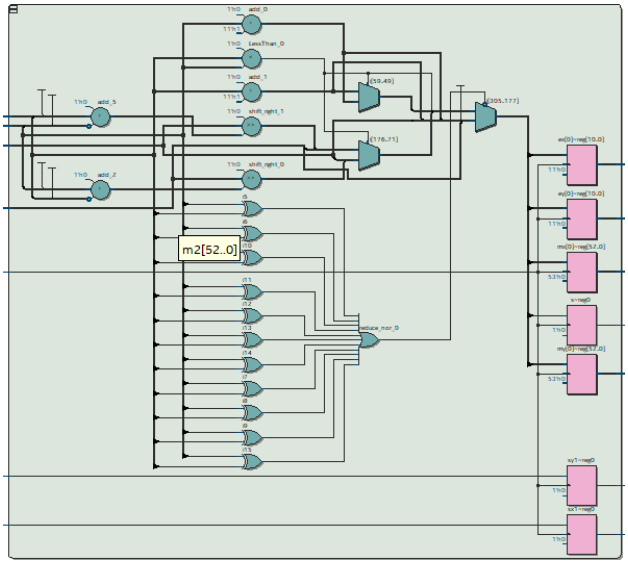

Fig.6.RTLSchematicofCompareandShiftblock

B. ReversibleAdder/SubtractorUnit

In order to perform the mantissa addition/subtraction a 52bit carry select adder has been designed using KMD gate 4.The52bitCarryselectadderconsistsofthreeseparateReversible Ripple carry adder (RCA). The first lower order 26bits is taken and given as the input to 26 bit RCA (RCA1) andthe lower order sum ranging from [25:0] is generated alongwith an output carry (C1). This Higher order bits from [51:26]is given as the inputs to two separate RCA (RCA2 and RCA3)with each having its initial carry as 0 and 1 respectively. Thesum and carry results from RCA2 and RCA3 are multiplexedand selected based on the output carry (C1) generated fromRCA1. The structure of a 52 bit Carry select adder is shown infigure7.

C. ReversibleNormalizationunit and Roundingoff

The third stage of the RFPA is Normalization and roundingunit. The normalization step could be a left shift or a right shiftof the mantissa. If the left shift is required for normalizationthenleadingzerosmustbecountedbasedonwhichtheshifting will be carried out which in turn will decrement theexponent.

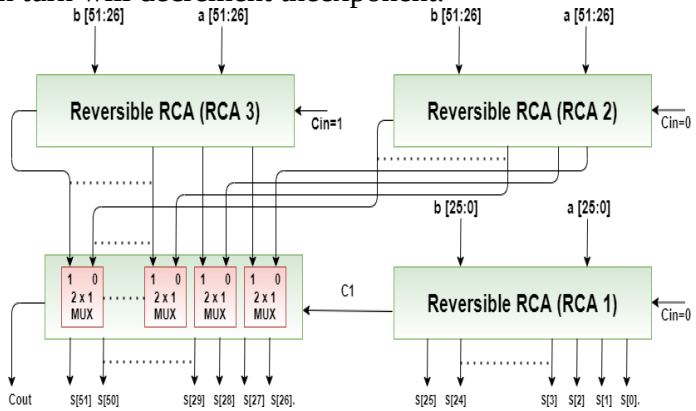

Fig.7 ReversibleCarrySelectAdder

Similarly if theright shift isrequiredfornormalizationthenthenormalizationunitshiftsthemantissabysingleposition which in turn will increment the exponent. This stepensures correct value of mantissa and exponent. Finally theroundingoffunitroundsofthemantissabasedonzeroroundingalgorithms.

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V. RESULTSANDDISCUSSION

ThePipelinedDoublePrecisionRFPAisdesignedandsimulated using Modelsim 10.7c.Parameters such as Power,Cell utilization, Timing and Maximum Operating FrequencyareanalyzedusingQuartusPrimeEdition20.2,10CX220YF672I5G device with respect to Cyclone 10 GXfamily.

A. SIMULATIONOFPIPELINEDRFPA

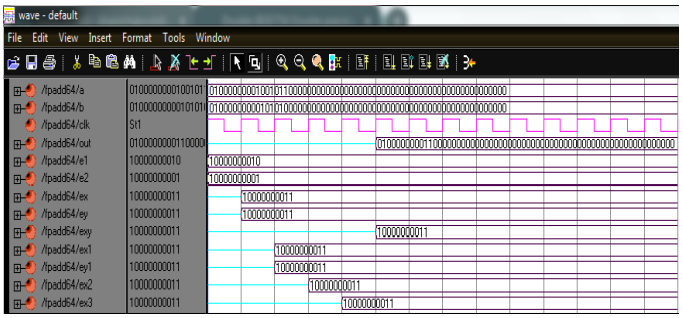

Fig8.Simulation resultofRFPAasadder

The Simulation result of Pipelined RFPA as an adder is shownin theFig8. The Inputsfor the adderare +10.75and5.25given indoubleprecisionformat.Theresultobtainedhasbeen +16.

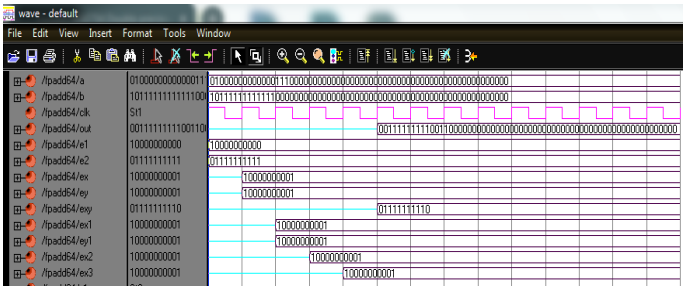

Fig.9.SimulationresultofRFPAasSubtractor

The Simulation result of Pipelined RFPA as a Subtractor isshowninthe Fig9.TheInputsforthesubtractorare2.4375and-1.75givenindoubleprecisionformat.Theresultobtained hasbeen+0.6875.

B. RTLVIEWEROFRFPA

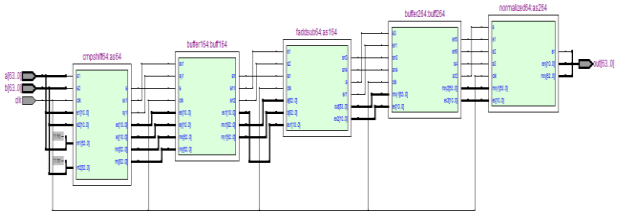

Fig.10RTLschematicofRFPA

The RTL schematic of Pipelined RFPA is shown in Fig 10after the post layout simulation. It can be seen in the there arethreemajorblocksnamelyReversibleCompareandShift,ReversibleFloatingpointadder/subtractorandReversibleNormalizationandroundingoffseparatedbybufferstoperformPipelining.

C. CHIPPLANNERVIEW

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TheChipPlannergivesthe visualdisplayofchipresources.

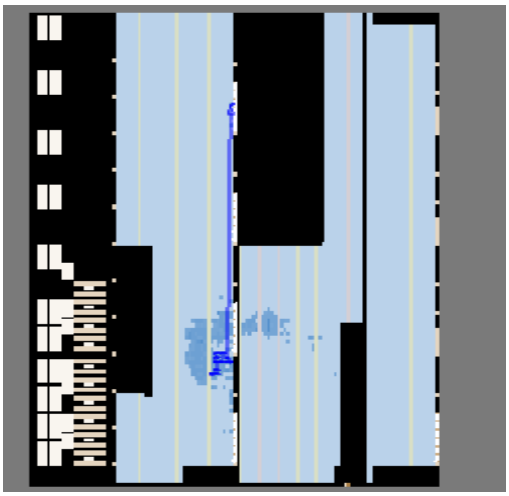

Fig.11ChipPlanner Viewof RFPA

Fig 11 is the view of RFPA in chip planner in which it showslogic placement, logic Block regions, resource usage, routinginformation, fan-ins and fan-outs, paths between registers, andhigh-speed transceiverchannels.

D. POWERANALYSISSUMMARY

TheTableIIshowsthecomparativestudyofpowerutilizationbetweenSinglePrecisionRFPAandDoublePrecision RPFA. It can be seen from the table that the totalpower dissipation has increased by 4.3% in Double PrecisionRFPA. Fig. 12 shows the graphical representation of DesignedRFPAarchitecture.ThegraphshowsthatSingleprecisionRFPA dissipates lesser power compared to Double precisionRFPAbecauseofthefactthat,duetoincreaseinthenumberof bits the switching activity (Dynamic power) of latter alsogets increased which in turn contributes to the total powerdissipation.

TABLE II. POWERANALYSIS

PowerAnalysis	**Single Precision (mW)**	**DoublePrecision (mW)**	**%of Dissipation**
Static PowerDissipation	1.71	4.73	63.84%
Dynamic PowerDissipation	5.82	9.21	36.8%
Core DynamicPowerDissipation	25.79	51.97	50.37%
Total PowerD	639.	668.26	4.3%

Annals of R.S.C.B., ISSN:1583-6258, Vol. 25, Issue 6, 2021, Pages. 2947 - 2957
Received 25 April 2021; Accepted 08 May 2021.

issipati on	49		

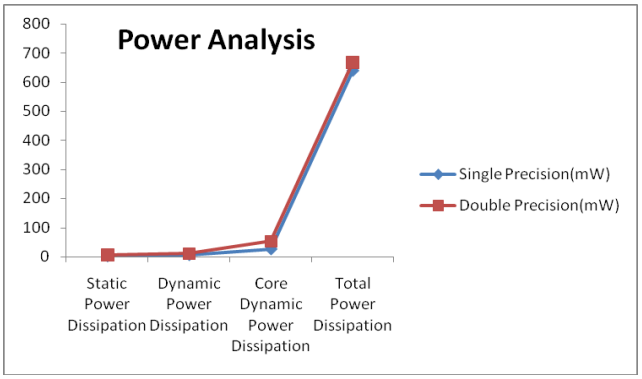

Fig.12Powerutilizationof RFPA

E. UTILIZATIONSUMMARY

TheTableIIIshowstheComparativestudyofSinglePrecision RFPA and Double Precision RFPA with respect tohardwareutilizationwhereasFig13showsthegraphicalrepresentationofthe same.

TABLE III. AREAUTILIZATION

Parameters	**SinglePrecision**	**DoublePrecision**	**% ofUtilization**
Logic utilization	596	2,042	71%
Totalregisters	265	513	48.3 %
Total pins	97	193	49.7 %

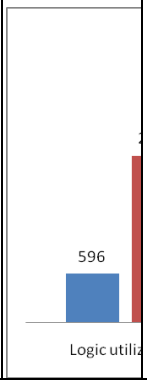

Fig.13ComparisonofUtilizationSummary

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ThetablisttheparameterscomparedforhardwareutilizationsuchasLogiccell,Registersandtotalpins.ComparingwithSinglePrecisionRFPA,DoubleprecisionRFPAutilizesmorenumberoflogicblocks, Registerandrequires as much as double the number of pins for input andoutputby71%,48.3%and49.7%respectively.

F. STATICTIMINGANALYSIS

TABLE IV. TIMINGANALYSIS

Static TimingAnalysis	**Single Precision (ns)**	**Double Precision (ns)**	**% ofImprovement**
Setuptime	0.093	0.089	4.3%
HoldTime	0.030	0.022	26.66%
MinimumPulsewidth	1.339	1.146	14.4%

The Table IV shows the comparative Static timing analysisforSingleprecisionRFPAandDoubleprecisionRFPAwhereas

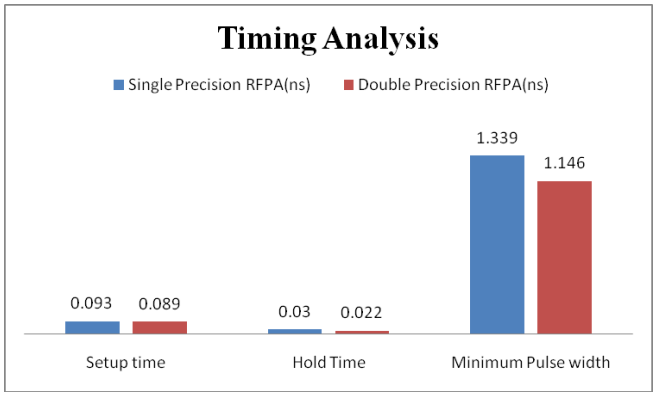

Fig.14ComparisonofTimingAnalysis

The Fig 15 shows the Graphical representation of Minimumpulsewidth required for designed Pipelined RFPA.Fig 14shows the graphical representation of the same. The setup timeis the minimum amount of time before the active edge of theclock that the data should be stable. Similarly, Hold time isdefinedastheminimumamountof time aftertheclock'sactiveedgeduringwhichdatamustbestable.Fromthegraphit can be seen that there is considerably improvement in setuptime, hold time and Minimum pulse width by 4.3%, 26.66%and 14.4%respectively.

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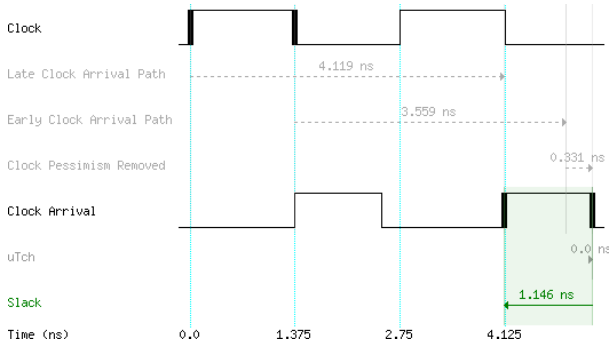

Fig.15GraphicalrepresentationofMinimumPulseWidth

G. MAXIMUMOPERATINGFREQUENCY

TABLEV. MAXIMUMOPERATINGFREQUENCY

Parameter	SinglePrecision(MHz)	DoublePrecision(MHz)
MaximumOperatingFrequency	333.33	370.3

TheTableVshowsthecomparativestudyofMaximumoperatingfrequencySinglePrecisionRFPA andDoublePrecisionRFPAwhereasFig16showsthegraphicalrepresentationofthesame.Thegraphicalrepresentationshowsthatthemaximumoperatingfrequencyof Doubleprecision RFPAhasincreasedby afactorof1.1comparedwithSingle precisionRFPA.

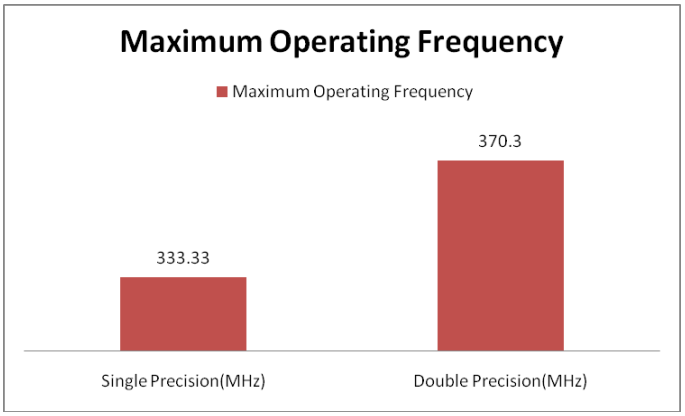

Fig. 16 Comparison of Maximum Operating Frequency in differenttechnologies

VI. CONCLUSION

Speed of Operation and area reduction is perhaps the majorconcern in most of the DSP applications. This paper presentsaPipelinedRFPMwhichusesIEEE754standard.AllmodulesofpipelinedRFPMhavebee

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ndesignedandsimulatedusingModelsim10.7c.Theparameterssuchasarea,power,cellsutilizatio nandmaximumoperatingfrequencyhasbeenanalyzedusingcadencegenussynthesis 14.25 on 180nm and 90nm technology,in which PipelinedRFPM with 90nm technology shows better improvement intermsofArea,Cellsoccupiedby67.17%and4.42%respectively while Maximum operating frequency by a factorof 2.73. The designed RFPM can be used for High speed DSPapplicationssuchasFastFourierTransform,QuantumComputingandOptical Computing

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