High-Speed Area-Efficient VLSI Architecture of Three-Operand Binary Adder

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Abstract

Addition is one of the basic functions of mathematics. It is widely used in many VLSI applications such as the construction of specific DSP applications and microprocessors. Additionally, this adds two binary numbers, it is the core of many mathematical functions such as subtraction, multiplication, division, address counting, etc. The purpose of this project is to propose a modification of a new gateway level, to design three operand adderSum based on acquisition of the additive used to design three operator-carrying adders. Therefore, a new and faster localized construction is proposed using a number-based prediction to make a triple binary adder that consumes very little space, low power and significantly reduces adder delay in O (log2 n).

INTRODUCTION

Today, Addition is the one which is used widely in mathematical function, and in almost all CMOS VLSI digital systems, such as DSP Processor, micro-processor, GPU consist of adder. For adding a multi-bit adder, multiplier, subtractor, etc. Full adder(FA) is the primary block.

Full adders are essential features in applications such as digital signal systems and general purpose microprocessors . For

many mathematical operations such as addition,subtraction, multiplication, division and address generation, this module is the basic component for the above operations. Therefore, full adder functionality will affect the full program entry. In addition, the explosive growth of laptops, cellular systems, and mobile networks has intensified research efforts on low-energy microelectronics. Therefore, today there is an ever-increasing number of portable applications that require low-power and high-capacity circuits. Therefore, in view of these issues, the construction of a full-scale expansion with low power dissipation and the effects of low delays are of great interest.

RELATED WORK

Narule et al. (2016) produced a floating point addition with operand with short delays.. The

internal width, which is particularly sensitive to delays, is made in compliance with IEEE Std-754. Leading zero anticipator (LZA) and a compound adder are used to refine the composition of the full type. Contrary to the three operand adder targeted, the proposed version reduces the delay by 7.79 percent.

Dave et al. (2007) suggested using common adder structure such as parallel prefix adders to achieve the installation of three operands. One of the advantages of this method is that it eliminates the need for dedicated adder units when performing three input addition.

Tsiaras et al. (2017) propose the process of entering multiple numbers into a Logarithmic Number System (LNS). The suggested method is based on setting the data to the highest input value. In cases of 4, 8, 16, and 11-bit lengths, the proposed multi-operand adders are integrated and tested for complexity and efficiency using a 65-nm library 0.9V UMC CMOS.

Liu et al. (2011) introduced a modern highspeed and efficient terminal design using a pre-calculated compound followed by carryprefix computing logic to make binary additions of three operators, using less space, using less power, and reducing adder delays to $O(\log_2 n)$.

Voicu et al. (2017) introduced two low-cost 3D Stacked Hybrid Adders with similar properties, paving the way for the production of fast-acting hardware hardware. According to the anticipated computation principle, an N-bit extension applied to the equivalent Klinked K is making two N / K-bit additions in each phase alike.

Kenney et al. (2005) introduce and evaluate three ways to make a quick decimal addition to multiple binary coded operands. When adding input operators, two strategies predict BCD correction values and accurate intermediate results.

Cilardo et al. (2014) propose a new method of constructing complete repetitive circuits based on speculation, a method that conducts slow but sometimes active use while only a circuit to correct multiple cycle errors in a rare error.

Efstathiou et al. (2013) proposed the implementation of a multioutput domino CMOS logic of an 8-bit Manchester carry chain (MCC) adder. Two different 4-bit chains carry the chains of this charm in the same way.

Esposito et al. (2015) suggest a new latency theory based on Han-Carlson parallel-prefix topology showing latency variation KoggeStonetopology . This paper explains how predictable latency startup add-ons can be categorized and introduces a novel error detection network that reduces the chances of error compared to previous methods

Bhattacharyya et al. (2015) introduced a hybrid 1-bit full adder design that combines CMOS and

logic of the transmission gate. Construction was initially introduced by 1 bit and then expanded to 32 bit. Cadence Virtuoso tools were used to install the circuit in 180- and 90-nm technology. Jiang et al. introduces a complete 12-bit transitionor based on low power multiplexer (MBA-12T). The region has no direct contact with power supply facilities, which has led to significant reductions in short-term energy consumption, in addition to declining exchange rates and new renewable energy. According to detailed comparisons of HSPICE, the latest add-on saves 26% more power than the traditional 28-transistor CMOS add-on, using less than 23% more power than 10 adders SERF [1] and 10T [4] and 64% is very fast.

PROPOSED SYSTEM

The basic unit for performing computational calculation is a three operand binary adder which is used on various cryptography and pseudorandom bit generator (PRBG) algorithms. Binary additions for three operand can be done using two adders or three operand adder. Carry-save adder (CS3A) is an efficient and widely used process for the addition of two binary operands in modular arithmetic used in cryptography algorithms [5] - [8], [12] - [14] and PRBG methods [9]] - [11]. However, delayed transmission loads in the CS3A loading phase have a significant impact on the performance of MDCLCG and other cryptography architecture on supported IoT devices. For reduction of delay, a parallel add-operand such as Han-Carlson (HCA) can also be used to add a binary operand to three operands.

Reduce critical delay delays in O (log2 n) sequence but increase location in O (n log2 n) [15].
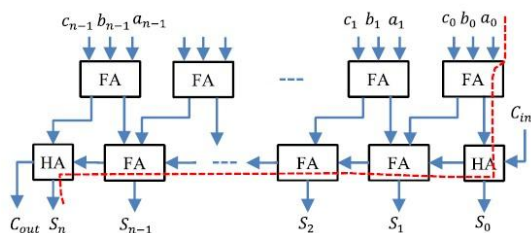

Fig. 1. Three-operand carry-save adder (CS3A).

Therefore, it is necessary to upgrade the active VLSI architecture to make binary operand binary additions with hardware resources.

A new high-speed approach used in a highspeed adder technique is proposed to make a practical addition to the project that consumes more gate space while reducing propagation delays compared to a standard adder Carry-save adder (CSA) is a widely used procedure to make triple binary adders It includes the addition of three operators in two stages the first stage is the collection of full adders. Each complete addition includes a bit of "carry" and "sum" simultaneously from the binary input ai, bi and ci. The second phase is a ripple-carry adder that combines the final size of the n-bit "sum" and the onebit size "carry-out" signals when the addition of three operand is released. The "carry-out" signal is still propagated by the number of full adders in the ripple-carry stage Therefore, the delay increases in proportion to the increase in the bit length. The architecture of a threeoperand carry-save adder and critical path delays depends on the carry propagation delay of ripple carry stage and are evaluated as follows,

$TCS3A = (n + 1) TFA = 3TX + 2nTG$

Similarly, the total area is assessed as follows,

ACS3A = 2nAFA = 4nAX + 6nAG

Here, the AG and TG show the local delay and distribution of 2 basic input gate (NO / OR / NAND / NOR) respectively. AX and TX show area delays and propagation of 2 XOR input gate respectively. The biggest problem with CS3A is significant delays of critical pathway increasing with increasing bit length. This delays in the critical distribution method influences the overall delay of the integration of modular arithmetic based cryptography with PRBG, of which the three-operand adder is the main base.

SUM BASED ADDER

• Three operand carry save adder can be designed by sum based carry
   finding adder

In sum based adder

Sum S = a xor bxor c and

 Carry = a.c + b. S

So we need one three input XOR gate ,two AND gates , one NOT gate to perform the addition operation. Therefore it reduces the time consumption.When comparing to other adder circuits , this type is very helpful in reducing the area overhead
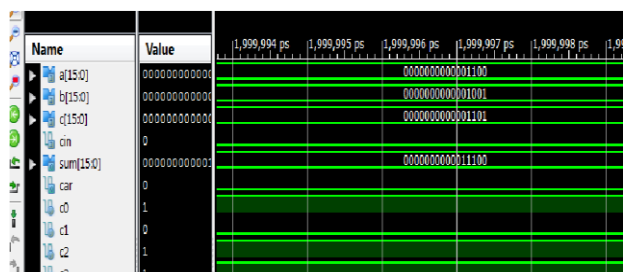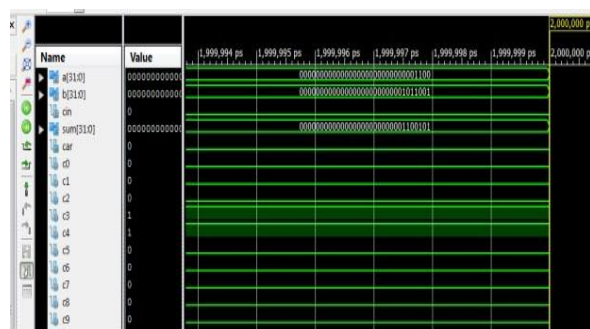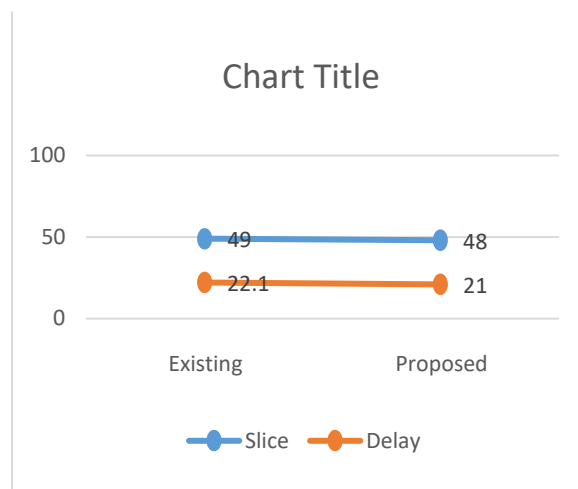

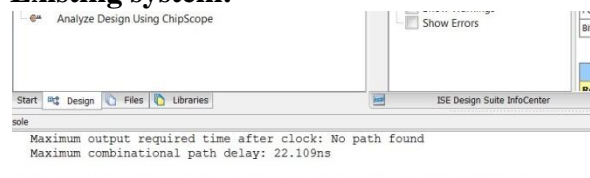Figure: Output of three operand addition

Fig. 32 bit addition

SIMULATION RESULTS
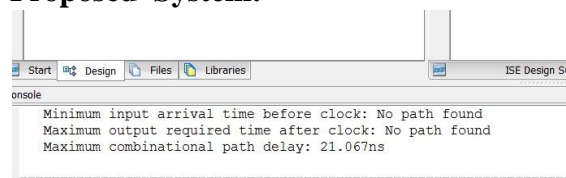
Existing system:

```
          Analyze Design Using ChipScope                    Show Errors              Bit

Start    Design    Files    Libraries                        ISE Design Suite InfoCenter
sole
   Maximum output required time after clock: No path found
   Maximum combinational path delay: 22.109ns

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```

Proposed System:

```
Start    Design    Files    Libraries                        ISE Design Su
onsole
   Minimum input arrival time before clock: No path found
   Maximum output required time after clock: No path found
   Maximum combinational path delay: 21.067ns

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By using Xilinx 12.1i we can able to obtain the simulated and the synthesis report for the propsed system.

In the table 7.1 we can able to find the various parameters used in the propsed and existing system by using spartan-3 processor

s.no	Parameter	Existing	Proposed
1	Slice	49	48
2	Delay	22.1	21

The change in time and area for the proposed and existing system based on the implementation which is done by Spartan 3
processor in shown in the given table. When compared to existing system the newly proposed system significantly reduces the area consumption

CONCLUSION

In this project ,High speed area efficient adder method and it's VLSI architecture are proposed inorder to perform the three operand binary addition for its efficient computation of modular arithmetic.These are very much used in cryptography and PRBG applications . This method is a sum based carry adder which means the carry in terms of summ which is used to calculate the carry of the input.he main change of the newly proposed architecture is the reduction of delay and area in the prefix computation stages in PG logic and bit-addition logic that causes to an overall reduction in critical path delay, area-delay product (ADP) andpowerdelay product (PDP)

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