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Fast and Power Efficient Voltage Level-Up shifter Using Dual Current Mirror Technique

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ABSTRACT

In modern days the dual supply voltage methodology is used widely in VLSI design in order to minimize the power dissipation. The conversion from the low to high voltages Level shifters are plays a pivotal role. In this article we proposed a low power and energy efficient level shifter using Wilson current mirror level shifter. The suggested design was implemented in cadence tool with 45nm technology. A power consumption of 2.613nW and a delay of 861.3pS was observed to translateasource voltage of 0.3Vto 1V at 1MHz in 45nm technology.

Keywords:
Dual-Supply,Level-Shifter, Current Mirror, Power Consumption.

Objectives of the Proposed Work
To get a low latency, power efficient output and it is analyzed.
To develop the efficient circuit with low static power is observed.

Motivation
Level shifters are widely used in interfacing devices. For interfacing other logics are required.To avoid any additional integrated logics we shifted to level shifters. In which we can translate the logic levels without any additional integrated logics.

Methodology
The proposed circuit is designed by using Wilson current mirror principle. By this technique we have measured the power and delay parameters. As, we promised the results obtained are efficient than the existing circuit.

Introduction

The world is shifting towards technology more rapidly. In earlier days the size of electronic gadgets was large compared to the same gadget at present. The size of computer when it was discovered was very vast that it occupied a large area but now the same computer is such small that it can be carried anywhere with ease. The main reason for this drastic change, is the advancements in the electronic industry. Transistors played a key role in this changing the world of electronics. In recent years the size of transistors, was reduced which resulted in the shrinkage

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in the size of the gadgets. As the size of the transistor is getting reduced the power dissipation is the main area of concern. There are various techniques available to minimize the power consumption of the topology. To minimize the power intake in CMOS topology the Source voltage reduction is one of the best technique. One of the major techniques which uses this scaling of supply voltage and has a high rate of success in multi-supply . In multi-supply technique there are two supply voltages. The major part of the circuit operates at nominal supply voltage ie VDD generally known as VDDH, and the non-critical portion of the circuit operateson the voltage which is less than the supply voltage known as VDDL. By using this technique, the dynamic power of the circuit is reduced without altering the performance.

Literature survey

Level shifter is defined as an interfacing circuit which is used to translate signals from one logic level or voltage level to different voltage level, allowing compatibility between integrated circuits (IC's) with different voltage requirements. The major application of level shifter is found in digital trails and SOC (system on chip) where distinct units or sub units operate at numerous voltages and speed. It can be used an interfacing element in between two voltage domains. To correct the supply voltage levels for consecutive digital blocks in dual supply architectures the Voltage Level Shifters are plays a key role.

The application of level converter was experimented on flip-flops to find the circuit heftiness against supply which is a key factor that differentiates better level converter model. The level shifter was designed using the multi-supply technique and two stage cross-couple technique [2] was used to design the pull-up network. For the 1st stage of pull-up network an additional PMOS were connected in parallel to upgrade the stability of the pull-up network. The topology was designed using 90nm CMOS technology. This circuit could adapt 100mV to 1V. For a 200mV input signal static power dissipation of 8.7nW, a propagation delay of 8.7nW and a total energy per transition of only 77 fJ at 1 MHz the LS was designed using the Differential Cascade Voltage Switch (DCVS) technique [3]. At the output stage a Split inverter was used to minimize the power intake. The design was implemented in 180 nm CMOS technology. This design can covert the lowest input signal of 100mV input signal to 1.8V. For an input of 400mV to shift to 1.8V the propagation delay was 31.7 ns, average static power of less than 60 pW and energy per transition was 173 fJ. The pull-up network of the level shifter was designed using a regulated cross-couple (RCC) technique [4]. The post layout simulation was performed using 180nm CMOS technology. This level shifter could translatefrom 80mV to 1.8 V. For an inputfrequency of 1 MHz the power dissipation and propagation delays are 123.1 NW and 23.7 ns respectively. A new configuration of voltage level shifter which can perform both level-up and level-down shifting operations. It uses transmission gates and a multiplexer[5] in which input voltage acts as select line and supply voltages as input lines, rest of the circuit is used for either up conversion or down conversion. The proposed topology can be used for low power and immense speed applications. It can up/down convert from 0.4V to 1V and vice versa. A new voltage level shifter which uses hybrid combination of Wilson current mirror and CMOS logic gates. It was designed for Dynamic voltage scaling (DVS) applications [6]. Five qualities involved in designing the new level shifter were (a) smaller area in terms of layout for sub threshold voltage changeover, (b)low power dissipation in above threshold operations, (c) balanced rise and fall time delays in operating range, (d) transistor sizing and threshold voltage parameters are insensitive to operating range, (e) bidirectional level shifting operations. Hybrid buffers, current mirrors and delay circuits were

used in this work to boost the performance of the level shifter in terms of power, delay and duty cycle over full range of DVS applications. A circuit that has no cross coupled connection [7] which leads to diminution in delay. Transmission gates are used in designing the proposed level shifters. Stable duty ratio and High-speed performance features the configured level shifter to become suitable for wide I/O interface voltage applications in ultralow power design using CMOS Technology.

A new configuration of voltage level shifters using modified Wilson current mirror circuit MTCMOS (Multi threshold CMOS) technique [8] were applied to Wilson mirror level shifters to reduce power intake, but there is a limitation of leakage power dissipation. By using the stack technique, the problem of leakage power dissipation is solved. By applying both stacked and non-stacked techniques to the modified Wilson current mirror based level shifter the comparison were made. Here, forcing methods were implemented for power reduction in the circuit. Proposed level shifter Modifies Wilson current mirror Hybrid buffer using forced PMOS method and without forced PMOS Method. Novel LS was designed that uses a modified Wilson current mirror hybrid buffer (MWCMHB) [9]. Foe full range conversions and bidirectional level conversion the modified Wilson current mirror hybrid buffer level shifter was designed. The complete range indicated that the supposed operating voltage can be deep sub threshold, which is close to the VDDL of digital circuits, and VDDH is the typical supply voltage defined in a transistor technology. The minimum input voltage for which the circuit could work was 200mV. The circuit was designed using 65nm technology. A design was implemented using Half-Latch-based technique along with the current mirror technique [10]. Single PMOS was used as a Current limiter. This design could not work for the values of input below 100mV. For an input voltage of 200mV at 1 MHz the propagation delay was 18.4nW, power consumption of 6.6nW and energy per transition of 93.9fJ.

A hybrid design of a level shifter was designed using the cross-coupled and the current mirror techniques [11]. The output of the level sifter was taken using the split inverter which reduced the leakage current. This level shifter could only work till 330mV. For the voltages below 330mV this level shifter did not work properly. The internal level shifter (ILS) is designed with the aid of input and output branches, those are comprised of a governable current source, a diode-connected transistor, [12]NMOS switch transistor and basic inverter.The gate terminals of the output stage were separated by the ILS. The diode connected transistor is acts as input to the output inverter for the designed circuit. The circuit simulation was carried out using 40nm and 180nm CMOS technology. The circuit consumed small energy of 4.2 fJ/transition with VDDL and VDDH of 0.35 V and 1.1 V, in that order the design implemented in a 40-nm technology. This could operate for an input voltage of 80mV in 180nm technology. For eliminating the high leakage currents and speeding up the fall transition for pass transistor [13] the reduced swing buffer design was used. The design could operate in sub threshold region. The level shifter was designed using the65nm CMOS technology. These LS could shift a 300mV signal to output of 1V with propagation delay of 7.5ns, leakage power of 2.64nW and energy per transition of 123.8fJ. The area occupied by the design was 7.45μm^2. An overview of how dynamic current generator [14] can be used to reduce static power dissipation by operating only during transition times when input and output logic levels do not synchronize to each other. Strength of pull up and pull down networks are kept at equilibrium in order to perform level shifting for extreme values of low input voltages which are below threshold voltages. This structure ensures that no static current

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flows in between supply rails. Current mirror logic and Differential cascade voltage switch logic (DCVSL) were used in designing the low power voltage level shifter. An Energy Efficient Sub Threshold Level Converter [15] has presented the power reduction techniques while converting from deep submicron input voltages to nominal output voltages. The implementation of the model includes multi threshold devices, multi supply, and level converting delay and extending minimum input voltages. This level shifter will efficiently and reliably convert up to 1.2VOperating range of supply voltage ranges between 188mV and 1.2V, which makes it suitable for both sub threshold and DVS operation. How total power dissipation can be reduced by using two techniques namely AVLS andAVLGwhich raises source potential and the ground potential respectively. This work focuses on reduction in active power, leakage power and threshold voltage by using AVL scheme. The results of this Voltage level shifter verifies the characteristic of low-power circuit which could be utilized in designing of low power applications.
The sub and Super Threshold Logic Cells are interfaced with Low Voltage Level Shifter [16], the novel approach in which the main transistors were body-tied. This approach adds additional connection which leads to increase in the energy consumption. The level shifter could convert from 0.35V to 1.2V. voltage level shifters are classified into 4 types (a) Dual supply voltage level shifter (b) single supply voltage level sifter (c) pass transistor half latch voltage level shifter(d)pre charge circuit-based voltage level shifter [17]. The crisis we need to crack in the dual voltage method is to decide to which node the minimal voltage should be applied to minimize the power or delay of the totaltopology. Low supply voltage can be applied to non-critical paths in the design such as input and output modules. High supply voltage can be applied to critical path such as memories high speed digital blocks. A number of common misconceptions have been clearly identified and debunked. Here we described an automated design technique by using two supply voltages to reduce the power. [18] To condensed power and supply voltage is demoralized in a clock tree. By Combining the both automated design technique and two supply voltages technique we can reduce the power by 47% in random-logic modules and by 73% in the clock tree. By Combiningthe above techniques, we applied it to a media processor chip. By using the Schmitt trigger structures the efficient on-off ratio can be significantly enhanced [19], which successfully reduced the leakage at gate node hence, the output level will stabilize. [20], thefunctionality of the multipliers will exhibit down to supply voltages of 84 mV–62 mV. For an 8x8 bit multiplier the supply voltage is gives as 62mVand the total power intake of the circuit is17.9nW which is operated at a frequency of 5.2 KHz.In digital design the quadratic relationship between supply voltage and consumption of power, by voltage scaling we can effectively reduce the dynamic power intake of the particular circuit.[21-22] by building the half latch structure for DCVS circuits it consumes negligible leakage current owing to its complimentary pull up and pull down networks.

Proposed design

The schematic of the proposed voltage level shifter is shown in the figure 1. The suggestedlevel shifteris developed with the aid of Wilson current mirror technique. The proposed structure of the circuit is composed with input inverter, a dual current mirror and an output inverter. The input branch consists of a CMOS inverter using low voltage threshold PMOS and NMOS transistors. The input inverter is provided with a low VDD. To convert the voltage levels, we required current limiters and pull up networks. The current limiters are designed by using PMOS. Pull up network consists of current mirror.The output branch consists of an inverter. The

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inverter is provided with a high VDD.

When the input is LOW MP1 is ON and MN1off this leads the transistors MN5 to ON as the gate of MP7 is connected to drain of MN5 so the MP7 gets turn ON this leads MP4 MP5 MP6 to turn ON. This results the node Q1 to charge to VDD. As the input of output inverter is high the output is low. So, the output is low as that of VIN.

When the input is HIGH then VINB will be LOW which turn off the MN5 transistor. As VIN is high the MN4 and MN3 transistors will gets turn on. The MN4 transistor is connected to the ground then the voltage at node Q1 is zero. The MN2 gate terminal is connected with node Q1 the MN2 transistor will turn off. The input of the output inverter is connected with the node Q1. As the node voltage is low the input of the output inverter is low which result the output as high same as VDDH.

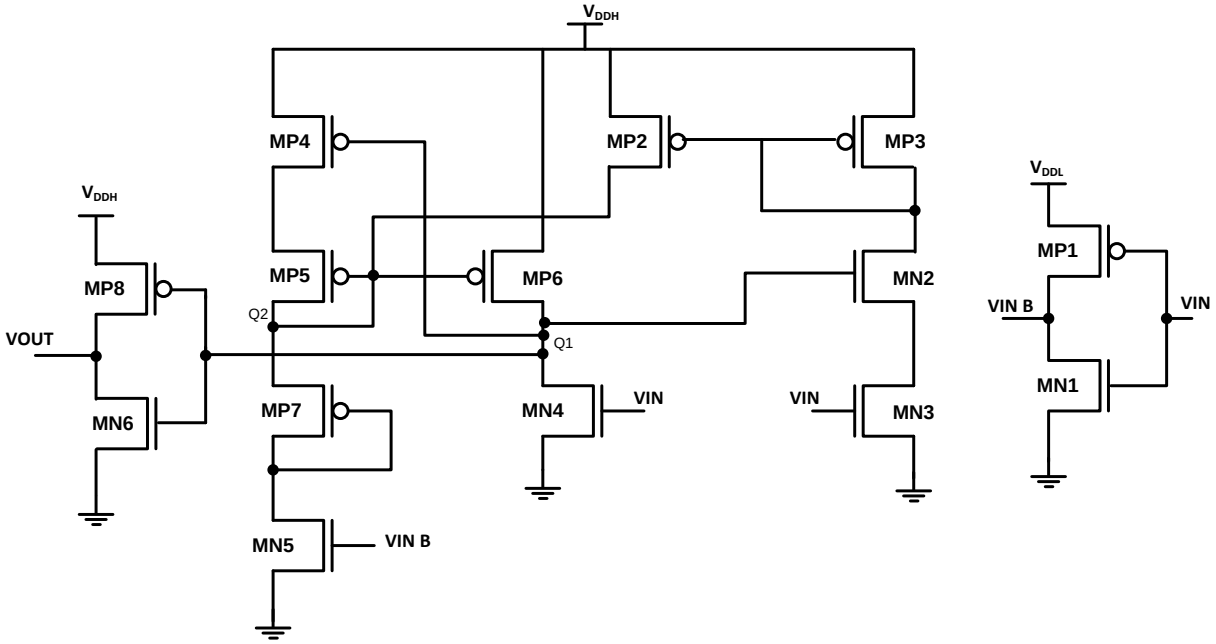

Figure 1: Proposed Level-Shifter

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Table1: Aspect ratio of the transistors.

Device	W/L(nm)
MN2,MN3,MN4,MP2,MP3,MP4,MP5,MP6,MN5	240/180
MN1,MP7,MN6	300/180
MP1,MP8	450/180

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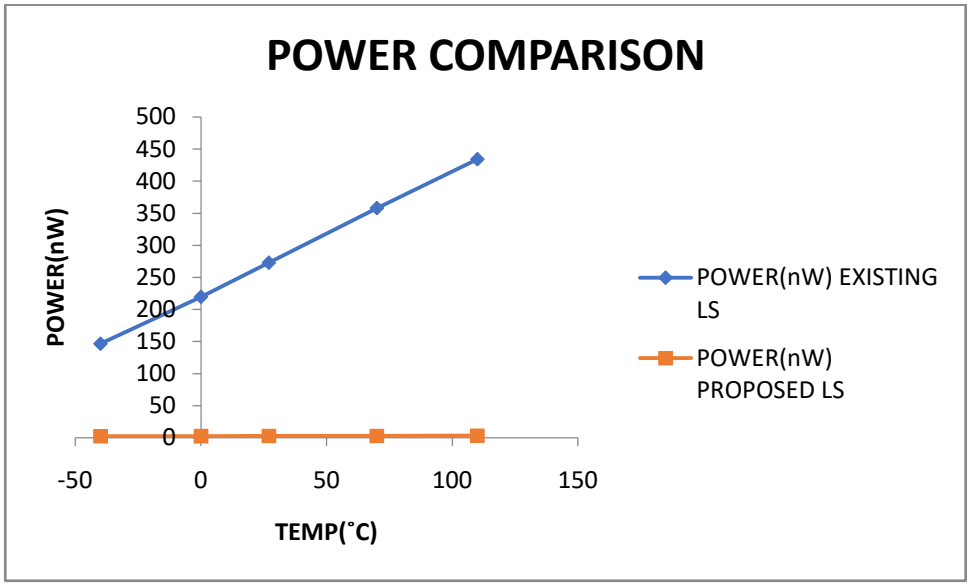
Results

The proposed LS was designed using 45nm technology. The proposed citcuit was compared with existed circuit[1]. Different analysis such as temperature analysis,frequency analysis and corner analysis were performed on both the circuits. At constant input voltage of 0.3v and constant frequency of 1MHz by changing the temperature from -40to110^{o}C temperature analysis was performed. Figure 2 show the variaison of the same circuit in two different technologies.



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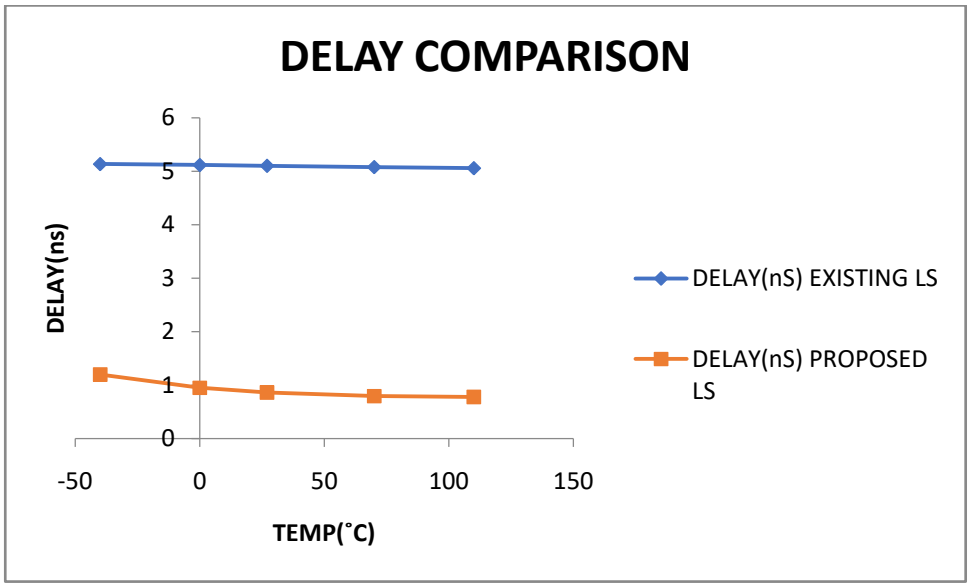

(b)

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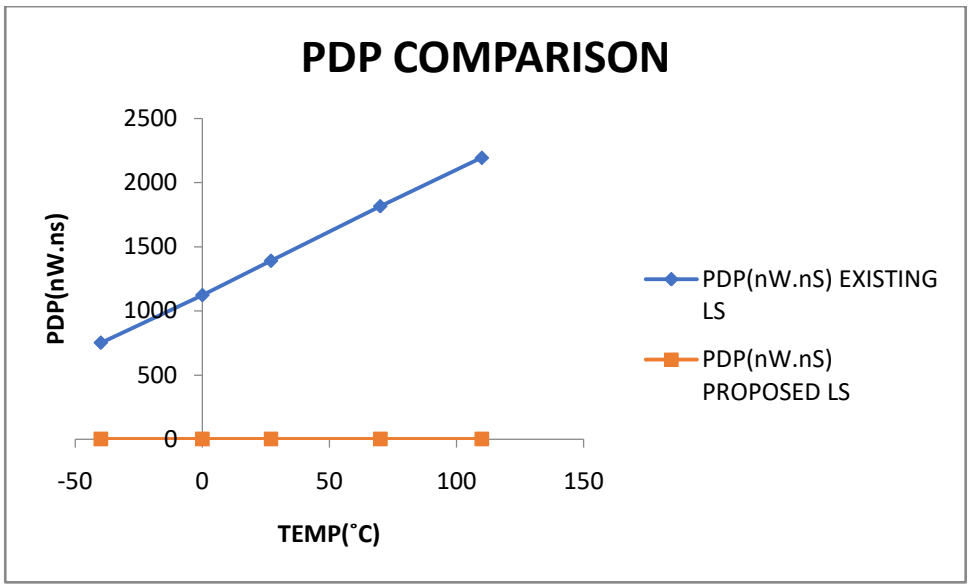


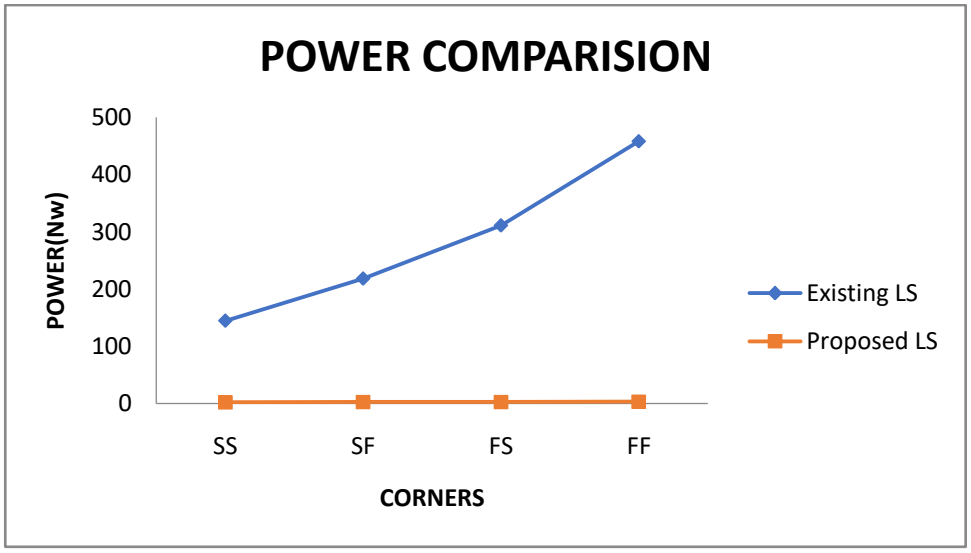
(c)

Fig . 2. a)Power, b)Delay and c)PDP comparison of proposed LS and existed LS[1] with change in the temperature of operation .

By enhanching the width of the transistor effects the power comsumption to increases and the delay of the transistor to decrease due to the reduction in the channel length of the transistor.

The LS desing was tested by changing speeds of the transistors.Power delay and PDP were calculated and the comparison was shown in figure 3.

By setting the input pulse train at 0.3V and the frequency of operation at 1MHz throughout the analysis the changes were tabulated. The observations were converted into graphical form for easy understanding of the viwer.



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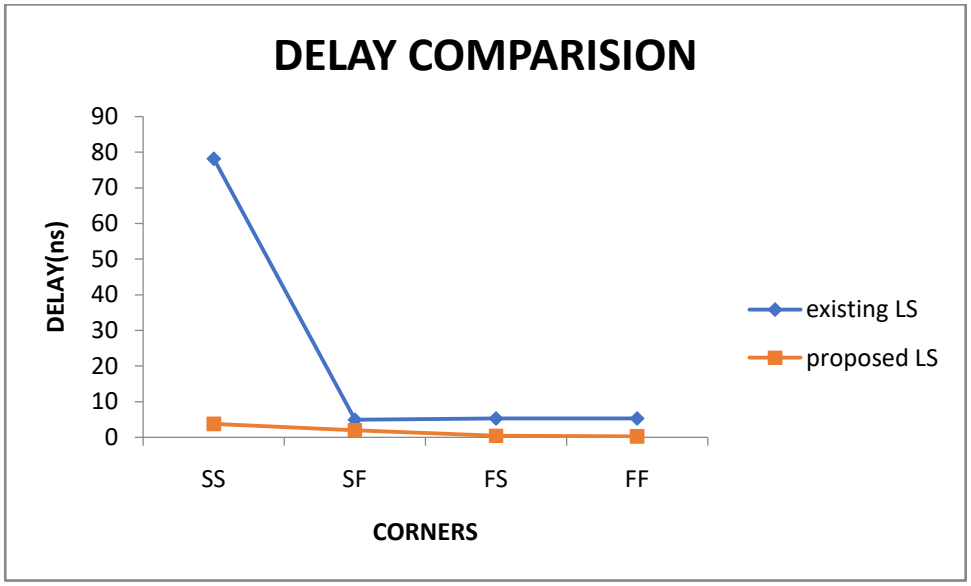
(a)



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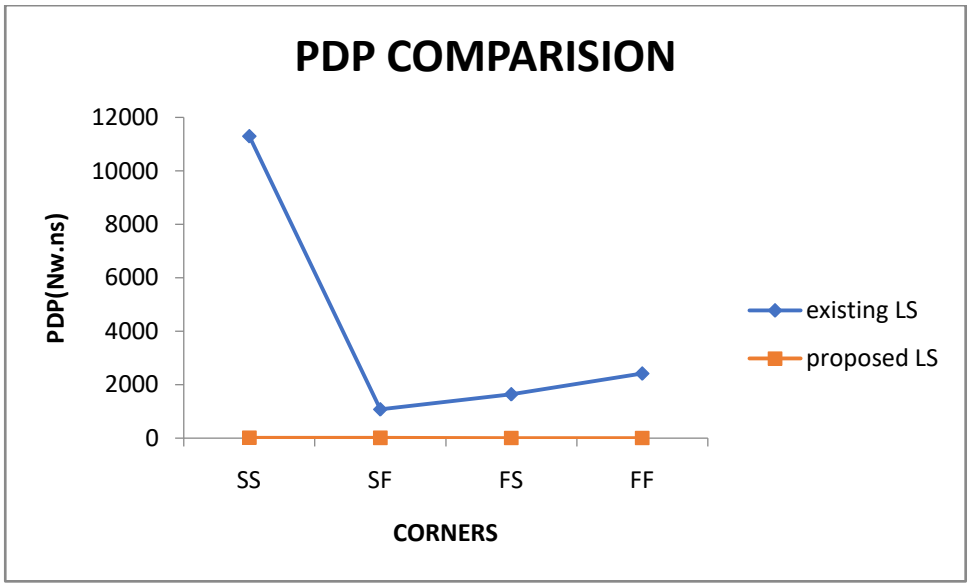

(c)

Fig.3. a)Power, b)Delay and c)PDP comparison of proposed LS and existing LS[1] with change in the speeds of the transistors.

The frequency was increased from 1MHz to 100MHz for an input signal of 0.3V and the variation in the parameters were depicted in the figure 4.

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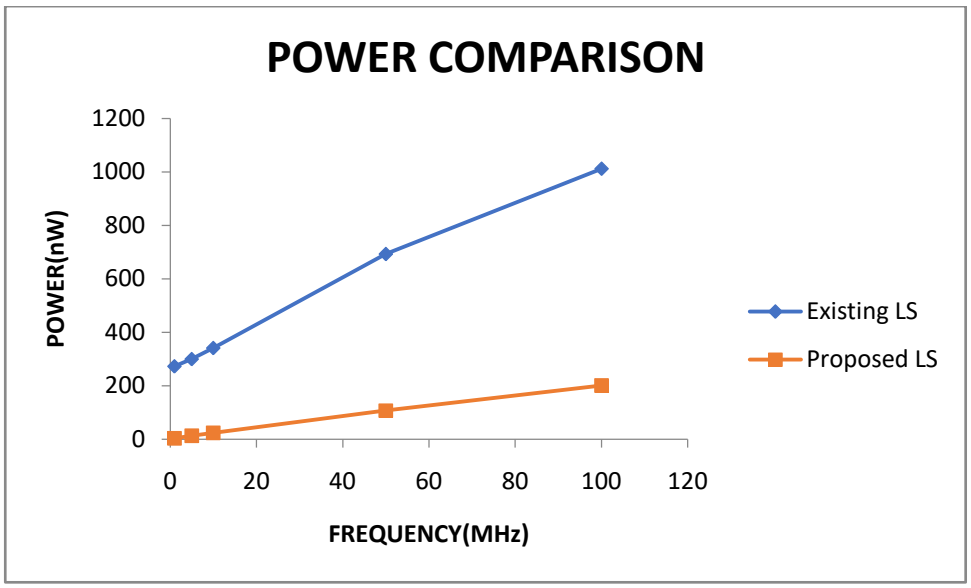
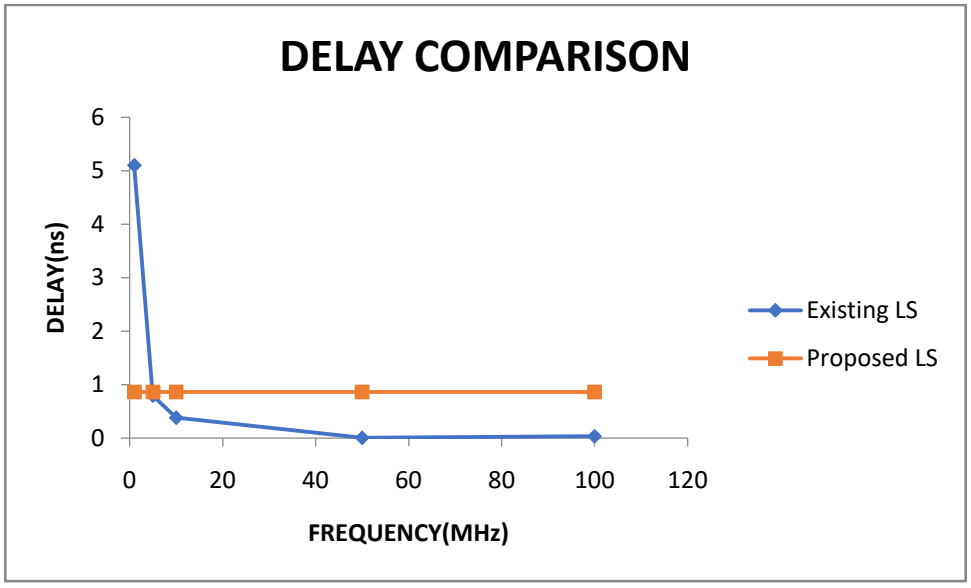


(a)



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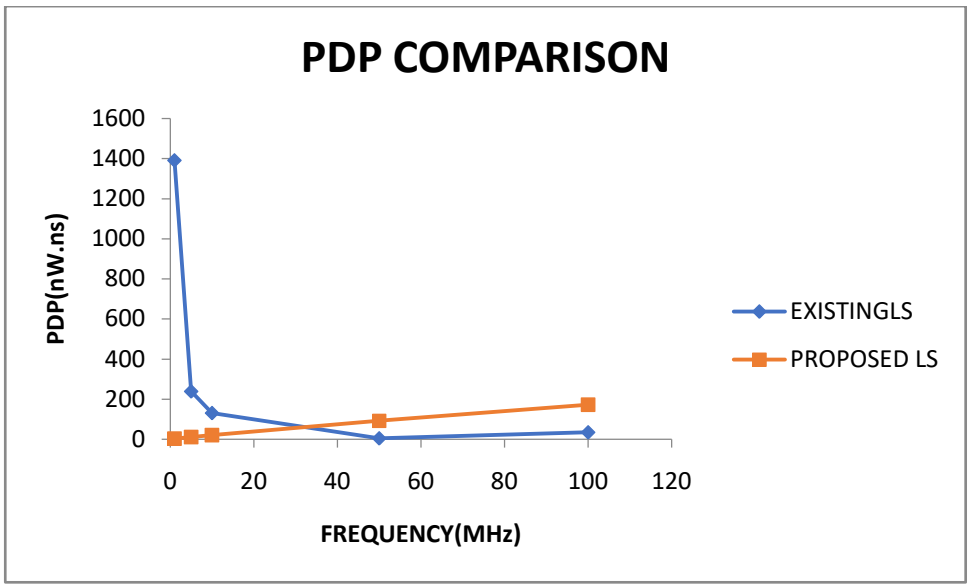

(c)

Fig. 4. a)Power, b)Delay and c)PDP comparison of proposed LS and existing LS[1] by changing the Frequency of operation.

As it can be observed that with change in the size of transistor has a great effect on the parameters while changing the frequency of operation.As that the power dissipation is directly depend on the supply voltage, frequency of operation and capacitance, hence increase the frequency leads power to increase.

Ref. process	Range	Transistors	Power(Nw)	Delay(ns)	Pdp(Nw.ns)
[1] 180nm	0.4-1.8v	08	76.34	6.1	465.674
[5] 90nm	0.1-1v	15	8.7	16.6	144.42
[6] 180nm	0.4-1.8v	14	60.05	31.7	1903.58
[7] 180nm	0.4-1.8v	12	123.1	23.7	2917.47
[9]90nm	0.1-1v	07	66.47	18.4	1223.048
P.LS 45nm	0.3-1v	14	2.613	0.861	2.249

Table.2. Comparison with other state-of-the-art level shifters

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Conclusion

A level shifter is used to convert the low voltages to high voltages. The level shifter is designed in this paper can convert the voltage ranging from 0.3v to 1v. The result is obtained with the aid of cadence tool in 45nm technology. The proposed design operated with a lower static power of 31.06pw in 45nm. As we promised that all the simulation results are accurate when compared with other designs while sustaining the same source voltage and frequency.

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