Annals of R.S.C.B., ISSN: 1583-6258, Vol. 25, Issue 5, 2021, Pages. 4637 - 4653

Received 25 April 2021: Accepted 08 May 2021.

A High-Performance Power Efficient Hybrid 2-4 Decoder Design

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ABSTRACT

This paper suggests a mixed logic architecture approach for implementing Low-Power, High-Performance Line Decoders. Most of the logic gates which are designed in ICs (Integrated Circuits) are by using CMOS circuits. These circuits are made up of blocks one is an nMOS pulldown block and the other is the pMOS pullup block and provide the best performance against device variations, area, and noise. The name Mixed Logic design (MLD) method combines the Pseudo-NMOS Logic with Dual Value Logic (DVL) for NAND/NOR Gates from Pass Transistor Logic (PTL), Transmission Gate Logic (TGL) for NAND/NOR Gates and CMOS logic, for implementing the Low Power (LP), reduced delay and High Performance (HP) decoders. Two additional topologies are added to the 2:4 decoders: 14-transistor Low-Power Topology intended to reduce power dissipation and a 15-transistor High Performance (HP) topology designed to reduce latency and energy dissipation while increasing performance by lowering the sum of transistors. With the above two topologies this paper also deals with a third design which involves the Pseudo nMOS Logic for designing a 2:4 Decoder with better performance than the above topologies. This design also supplies full swing capability. The logic design for 4:16 Decoder becomes easier by cutting the CMOS post decoder by using a 2:4 Decoder. This design method works for the Decoders both for with and without the Enable pin. Based on the results, we can draw a conclusion that the decoders implemented using Mixed Logic Methodology are ahead when compared to CMOS Logic design in all the constraints like power, delay, area, and performance with reduced transistor count.

INTRODUCTION

Complementary Metal-Oxide Semiconductor (CMOS) is indeed a form of MOSFET manufacturing procedure that includes complementary & a well-balanced n-type and p-type group of MOSFETs for logic devices. Microprocessors/microcontrollers, memory chips, as well as other digital functional circuits are mostly developed utilizing CMOS process. Image sensors (CMOS sensors), data converters, RF circuit designs (RF CMOS), and completely sophisticated transceivers are all analogue devices that use CMOS technology.

Because of the rapidly evolving technologies in mobile communication and deliberation, which relies on a transferable power supply, creating low-power VLSI (VERY LARGE-SCALE INTEGRATION) designs has become a primary performance target. As opposed to advances in battery technology, advancements in semiconductor technology are very recent. The mobile device has a limited amount of power to work with. Such architectures are constrained by more constraints, such as low power, high speed, high throughput, and a small silicon region at a low cost.

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Significant advancement in VLSI technology, along with better reliability and dwindling, have necessitated the construction of low-power, high-speed, reliable method. In computing of good efficiency devices like μ_p/μ_c, DSPs, low power architecture is the most pressing problem [3]. A decoder is a multi-circuit that agrees a method that allows along with conversions to series of outputs. Line decoders are used in a diverse range of products, including memory array, address debugging, code demodulation, seven-segment displays etc. This paper proposes a new hybrid logical framework to evaluate a decoder with lower power, delay, and transistor count.

CIRCUITS FOR DECODERS: AN EXPLANATION

CMOS circuits are classified into two groups based on the clock. One is Combinational Circuit which does not have clock and Sequential Circuit hold a clock signal. Decoder is a combinational circuit that admits many inputs and produce substantial number of output signals; for a 'n' number of inputs, a Decoder emits '2^n' number of output signals. n:m line decoders are the decoder circuits constructed and studied in this article. and relation between input and output signals is $m=2^{n.}$ [1]

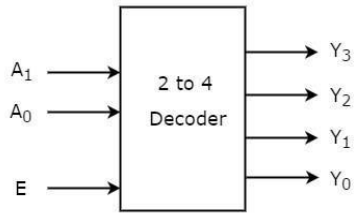

Figure 1. A 2:4 Decoder with 2 inputs, 4 outputs and an Enable pin.

2:4 Decoder Design Implementation

Decoder which takes two inputs and gives out four outputs is named as 2:4 Decoder. Relying on the inputs, one output will be active high at any given time for non-inverting Decoder. Table I encapsulates the logic function of a 2:4 Decoder, where A0 and A1 are the Decoder's inputs and Y0 to Y3 are the outputs produced by the Decoder. The Inverting outputs Y0 – Y3 are generated by an inverting 2-4 decoder, with only one output set to logic 0 (active low) at one time and logic 1 on the other 3 outputs. Table II encapsulates the function of an inverting 2:4 decoder. In traditional CMOS logic, NAND/NOR gates involve 4 transistors each, while AND/OR gates involve 6 transistors, the extra 2 for the inverter (NOT gate). As a result, in CMOS logic, NAND/NOR gates are chosen over AND/OR gates for implementing a high-efficiency logic operation. As drawn above in Fig. 2, an Inverting 2:4 decoder is designed using 4 NAND gates and 2 NOT Gates, accounts to a total of 20 transistors. Similarly, a non-inverting 2:4 decoder with a total of 20 transistors can be implemented using 4 NOR gates and 2 NOT Gates, as shown in Fig. 3.

TABLE 1. Truth Table of Non-Inverting 2:4 Decoder

A0	A1	Y3	Y2	Y1	Y0
0	0	0	0	0	1
0	1	0	0	1	0
1	0	0	1	0	0
1	1	1	0	0	0

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TABLE 2. Truth Table of Inverting 2:4 Decoder

A0	A1	Y3	Y2	Y1	Y0
0	0	1	1	1	0
0	1	1	1	0	1
1	0	1	0	1	1
1	1	0	1	1	1

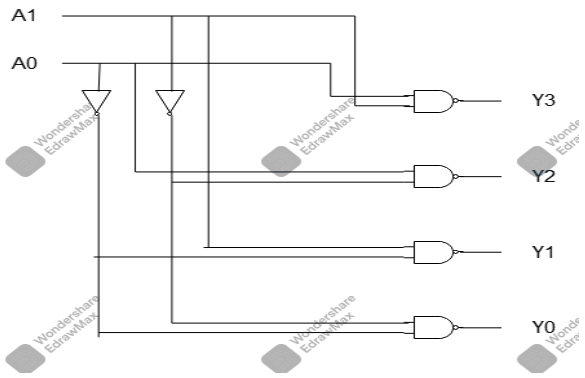

Figure. 2. 2:4 Inverting Decoder Gate Implementation.

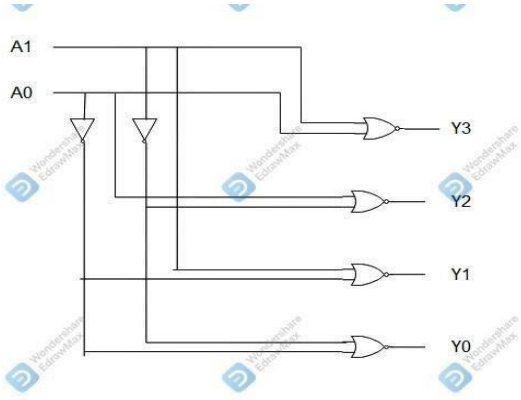

Figure 3. 2:4 Non-Inverting Decoder Gate Level Execution.

The Boolean functions for each output in the Truth table are indeed,

Y0 = A0'. A1' Y2 = A0.A1'

Y1 = A0'. A1 Y3 = A0.A1

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4-16 Decoder Design Implementation using 2:4 Decoder

4:16 Decoder acknowledges four inputs and gives out 16 output min-terms D0–D15 as shown in Fig 4. Four 4-input NAND/NOR Gates are needed to construct 4:16 decoder in CMOS logic.

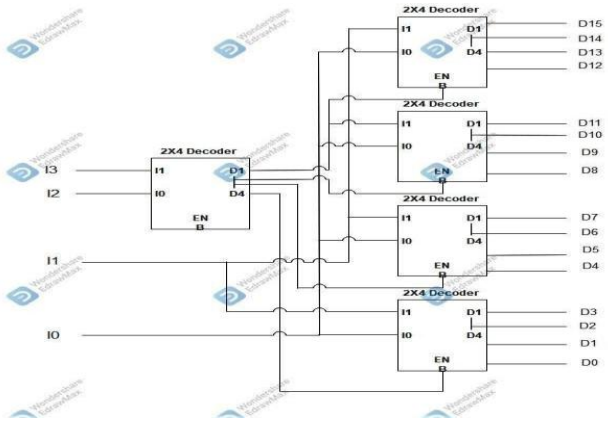

Figure 4. Block Diagram of 4:16 Decoder using 2:4 Decoder.

MLD METHODOLOGY

The Mixed-Logic is a combination of designs, including Dual Value Logic (DVL) from Pass-Transistor Logic (PTL), Transmission Gate Logic (TGL), CMOS Logic, and pseudo-NMOS logic. Because of its full-swung capacity, it has lower transistor count when compared to CMOS logic, and lower power and delay, we make use of this approach instead of traditional CMOS logic.[2]

Pass Transistor Logic

In conventional CMOS logic, the input is supplied at the gate terminal only, that is one of the failures of CMOS logic. Hence, Pass-Transistor Logic (PTL) is employed in place of CMOS principle to overcome this problem. However, with Pass-Transistor Logic, inputs can be given at both the drain and source terminals. CMOS Logic is a kind of logic that has been around for a long time., this improves field, strength, and speed.

For the design of these logics, there are two different circuit types. Complementary Pass-transistor Logic (CPL) is the first type, which uses only nMOS pass transistors. DVL and DPL utilizing both P-type and N-type pass transistors in the second process.[18] DVL is used in mixed logic decoder design, since it has benefits against DPL, such as fewer transistors and absolute swing capability, Fig. 5 and 6 write down two-input AND/OR gates implemented in DVL.

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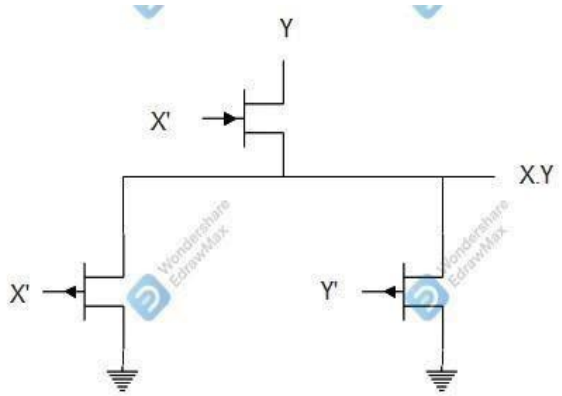

Figure 5. AND Gate implementation using DVL.

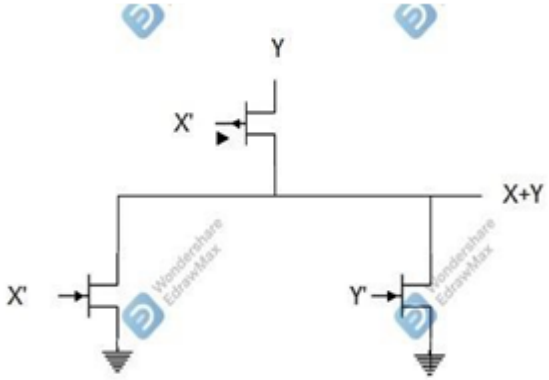

Figure 6. OR Gate implementation using DVL

Transmission Gate Logic

Transmission Gate Logic (TGL) which uses a Transmission Gate (TG) is a type of logic that is used to implement AND/OR gates. Decoders also have a benefit with the usage of these transmission gates. TGL logic gates have complete swing capability, but several input combinations are non-restoring. TGL based AND Gate as well as an OR Gate are also available. as shown below in Fig. 7 and 8.

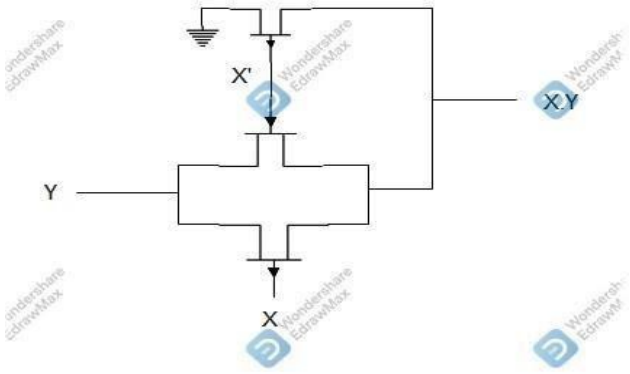

Figure 7. AND Gate implementation using TGL logic.

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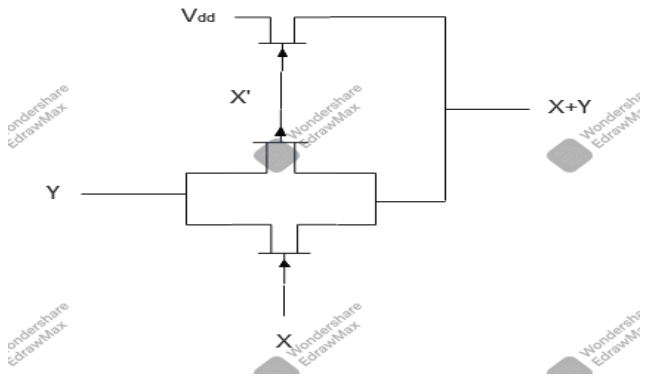

Figure 8. OR Gate implementation using TGL Logic.

Pseudo-NMOS Logic

A NOT Gate (Inverter) with gate terminal of pMOS transistor is rooted forever. A pull-down resistor is powered by the input signal. NMOS technology, which is like the use of a depletion load, is called as "Pseudo-NMOS". The network can be used in many CMOS logic circuits. In this case, pMOS will be linear for all the time. As a result of the low resistance, the RC time constant is tiny. The circuit receives a steady DC current while the motor is switched on.

CMOS p-channel is substituted for a lone PNP transistor with its gate rooted. The P-type MOS is still "on" because it is not guided by signals. The PMOS transistor sees V_{dd} as the efficient gate voltage. As a result, the p-type gate's overvoltage is still (V_{dd} –Vtp). When the N-block is turned on, a clear path is established between supply and field, and static power is extracted. The dynamic control, however, is lowered because of the lessen capacitive erecting.

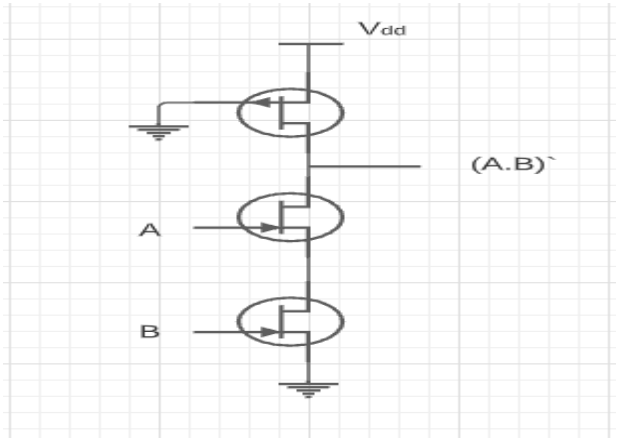

Figure 9. NAND Gate using Pseudo-NMOS Logic.

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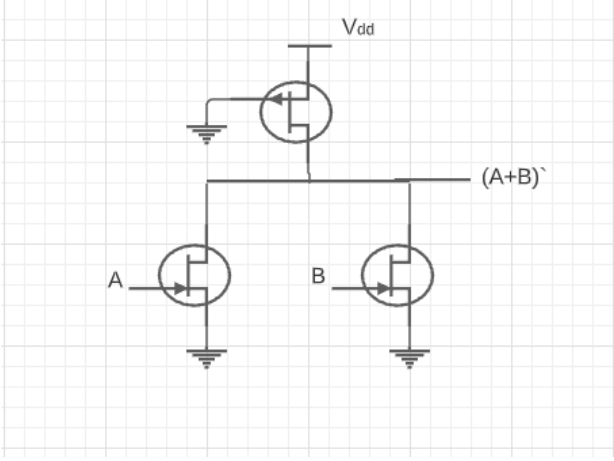

Figure 10. NOR Gate using Pseudo-NMOS Logic

DESIGN TOPOLOGIES OF 2:4 DECODER

As collated to CMOS Logic Design, the contemporary topologies for designing a 2:4 decoder for power-delay improvements with a reduced number of transistors of 14-transistor Low Power configuration for power reduction and a 15-transistor High-Performance configuration for delay reduction. The proposed topology, which has better performance than the current topology which uses a pseudo-NMOS logic to perfect area and increase speed of simulation, which has a lower number of transistors.

Existing Topologies

2-4 Decoder implementation using 14-Transistor Low Power Topology

Two NOT Gates and four NAND/NOR gates are needed in the design of an inverting ang non-inverting 2:4 decoder, a total of 20 transistors (4 for NOT Gate and 16 for NAND/NOR Gates) are used. However, by merging both TGL and DVL AND gates on one layout in place of NAND gate and choosing suitable control and generate signals, higher performance design can be carried out. Also, 1 of 2 NOT Gates might be removed, tends to result a configuration of 14 transistors (12 transistors for NAND gate and 2 for one NOT Gate). [2,7,9]

Consider the decoder's two inputs, let them be A and B, which gives four min-terms D0-D3. To eliminate NOT Gate of B. The first and third min-terms, D0(A'B') and D2(AB'), are designed using DVL AND Gates with A and B as the generated pulses. TGL AND gate is used to enforce the min-terms D1(A'B) and D3(AB), with B as the propagated signal for both min-terms. It is possible to remove the B NOT Gate with this selection of gates and inputs, results in a Low Power Decoder topology.

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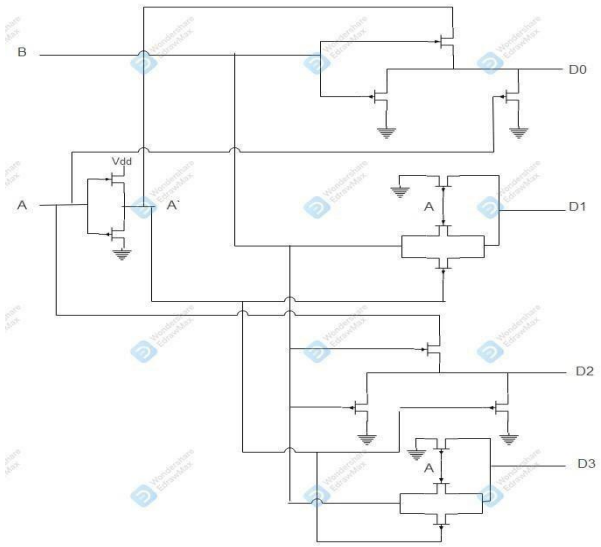

Figure 11. Design of 2:4 Decoder using 14-Transistor Topology

2-4 Decoder implementation using 15-Transistor High Performance Topology

The usage of complementary generated signal in min-term D0, the 14-transistor low power decoder design has the worst delay. This problem can be solved by using traditional CMOS logic gates to implement these min-term, as they do not need inverted inputs. To implement min-term D0, a CMOS NOR Gate is used with the inclusion of one more transistor in each topology. As a result of this change, the decoder design has three logics (CMOS, TGL, and DVL) precisely same as design, resulting an improved power and delay efficiency, and called the High-Performance (HP) configuration. [2,4,5]

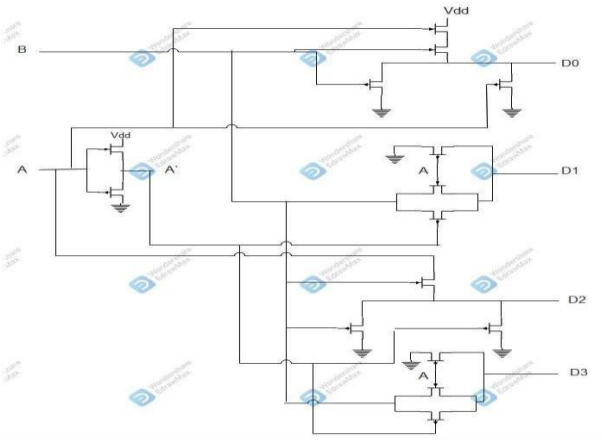

Figure 12. Design of 15-Transistor high performance Topology.

Proposed Design

The 14-transistor topology is Low power consumed and has less transistors than CMOS Logic, but it has a downside at D0 output: it has the worst delay at that output terminal. As a result, 15-transistor topology is constructed for better performance than 14-transistor topology by using a CMOS NOR gate at D0 terminal to reduce the delay.

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Apart from these, a better topology is designed than the 15-transistor logic, with higher efficiency, reduced latency, and efficient power consumption using only 14 transistors in the design. Instead of using a CMOS NOR gate in a 15-transistor topology, which increases delay to the circuit, a NOR gate with pseudo NMOS Logic is used, which is faster than a CMOS NOR gate and drops the need for the extra transistor in a 15-transistor topology.

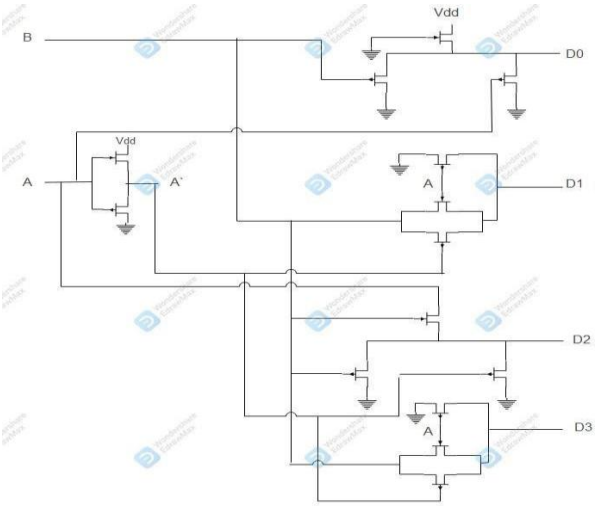

Figure 13. 14-transistor Pseudo NMOS logic.

MIXED LOGIC DESIGN METHODOLOGY WITH ENABLE

Using 2-4 decoder block which will reduce the transistors count in a n:2^n decoder. Using 2:4 decoders reduce design complexity and allows the construction of an elevating phase of decoder although they do not need any external logic gates. In the shaft-decoder, these logic gates were included. phases have many drawbacks, including increased wires and crosstalk because of interdependencies. Additionally, as n raises high, no. of logic gates also raises uniformly, enforcing up above on area.[12]

Decoder circuits are regulated to an additional enable input. The decoder only runs when the enable pin is running, lowering dynamic power consumption. Furthermore, in place of Gate level implementation, it is often recommended in modern chip design practices to create modules or sub-circuits which could be used relying on the situation.

TABLE 3. 2:4 Non-Inverting Decoder Truth Table with Enable

EN	A	B	D0	D1	D2	D3
0	X	X	0	0	0	0
1	0	0	1	0	0	0
1	0	1	0	1	0	0
1	1	0	0	0	1	0
1	1	1	0	0	0	1

TABLE 4. 2:4 Inverting Decoder Truth Table with Enable

EN	A	B	D0	D1	D2	D3
0	X	X	1	1	1	1

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1	0	0	0	1	1	1
1	0	1	1	0	1	1
1	1	0	1	1	0	1
1	1	1	1	1	1	0

The basic non-inverting CMOS 2:4 decoder with enable pin calls for three input NOR gates and three NOT Gates, total of 30 transistors. The DVL AND Gates can be used to construct D0 and D2 in the Low Power (Fig. 14) decoder, with A as the propagating signals and Enable pin, B as the controlling signals. TGL AND gates with B as the propagating pulse and A, enable as the controlling signals are used to enforce the min-terms D1 and D3. Two NOT Gates with the cumulative number of 26 transistors are essential for the 2-4 LP (Low Power) Decoder. The High-Performance decoder (Fig. 15) can be built by supplanting D0 min-term with a 3-input CMOS NOR Gate, which requires an extra transistor at D0, completing the total count to 27. For efficient output and lower transistor count, the proposed pseudo-NMOS design (Fig. 16) replaces the CMOS NOR gate with Pseudo-NMOS Logic at D0.[16]

The 4:16 decoders with enable are built with 5 2-4 decoders and no additional logic gates or transistors. A basic CMOS 4:16 decoder requires 150 transistors, while 4-16 Low Power decoders require 130 transistors, and 4-16 High- Performance decoders require 135 transistors.

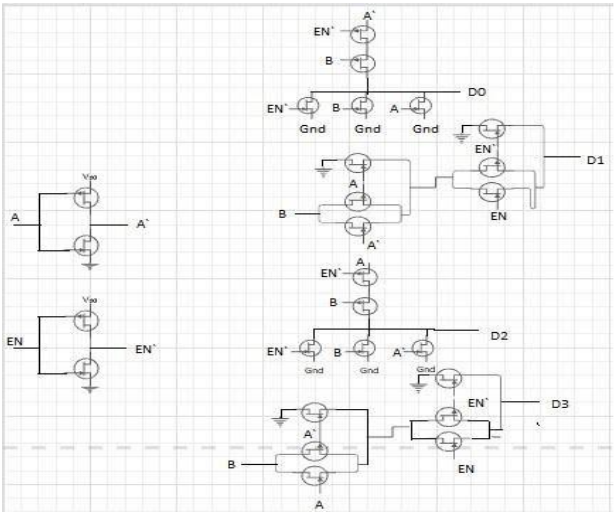

Figure 14. Design of 2:4 Low Power Decoder with Enable.

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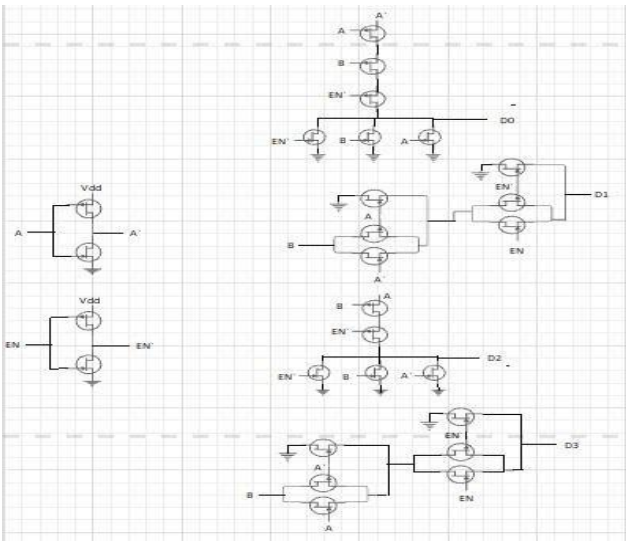

Figure 15. Design of 2:4 High Performance Decoder with Enable.

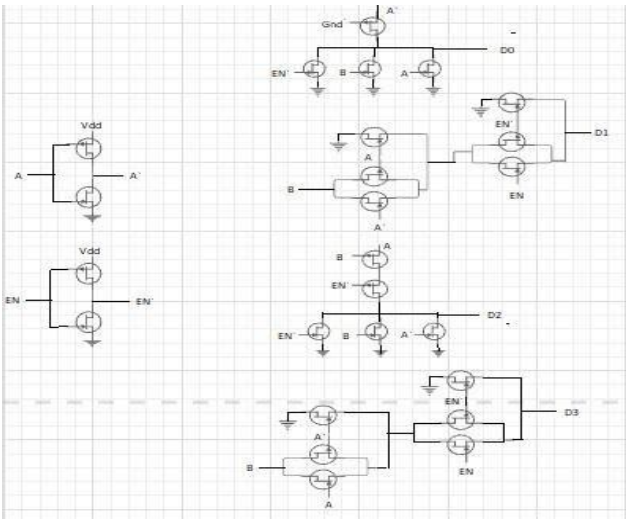

Figure 16. Design of 2:4 Pseudo-NMOS Logic with Enable.

SIMULATION AND RESULTS

The circuits are designed using the Cadence Virtuoso tool in 90nm technology, and the outputs acquired for the modern architecture approach decoders were drafted alongside the outcomes for CMOS decoders. In this model, 2 different innovative topologies are introduced, including one for power reduction another for increased efficiency, and one is proposed for reduced power and high reliability by using Pseudo-NMOS logic. In this scenario, the overall power of the circuitry as well as the delay are evaluated. The circuits are controlled by a 5V supply voltage.

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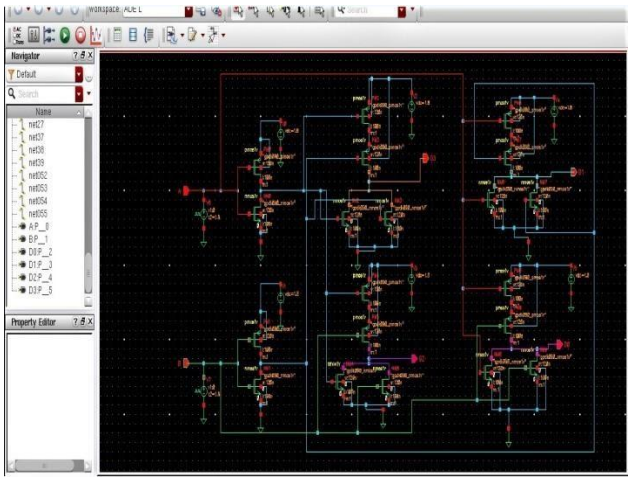

Figure 17. CMOS Logic Design of 2:4 Non-Inverting Decoder.

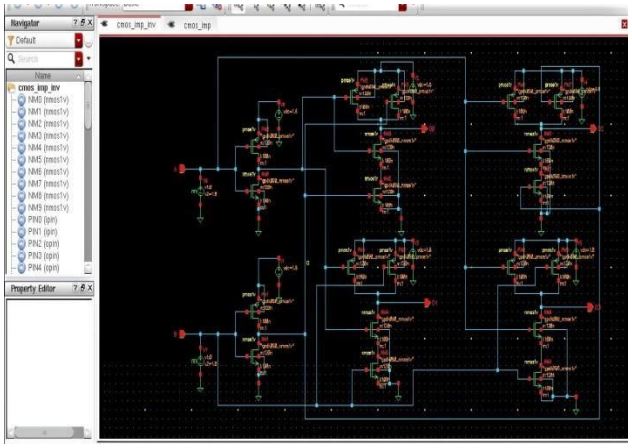

Figure 18. CMOS Logic Implementation of 2:4 Inverting Decoder.

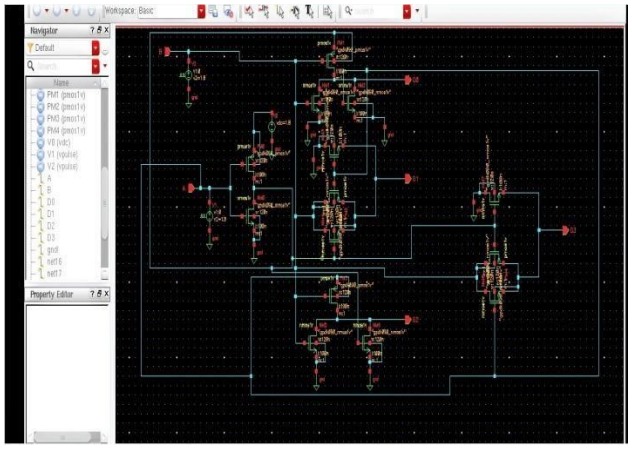

Figure 19. 14-Transistor Topology for 2:4 Non-Inverting Decoder.

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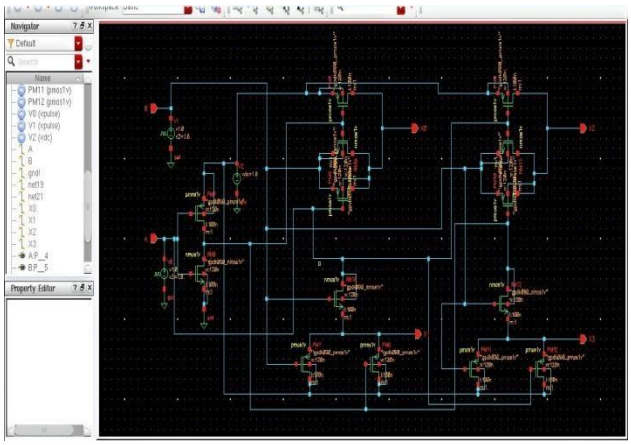

Figure 20. 14-Tranisistor Topology for 2:4 Inverting Decoder.

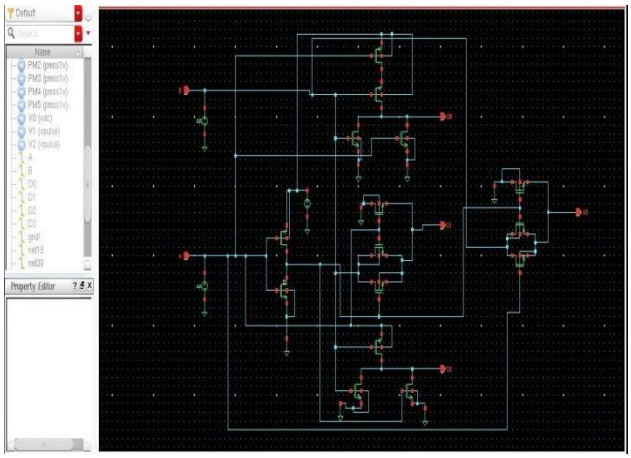

Figure 21. 15-Transistor Topology for Non-Inverting 2:4 Decoder.

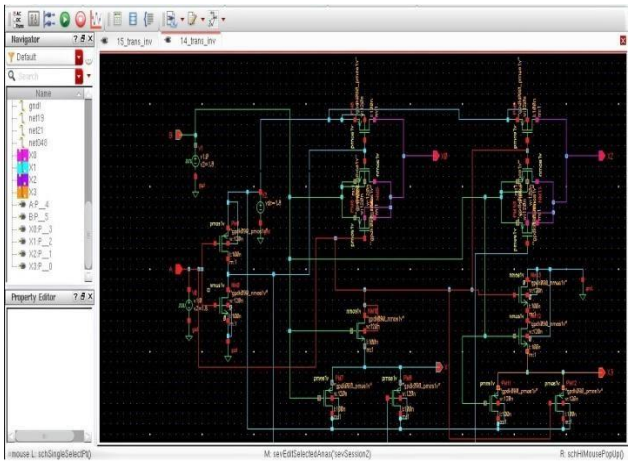

Figure 22. 15-Transistor Topology for Inverting 2:4 Decoder.

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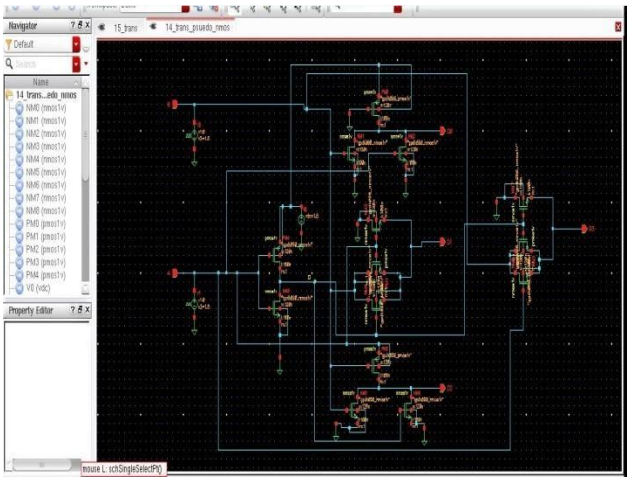

Figure 23. 14-Transistor Pseudo-NMOS Logic for 2:4 Non-Inverting Decoder.

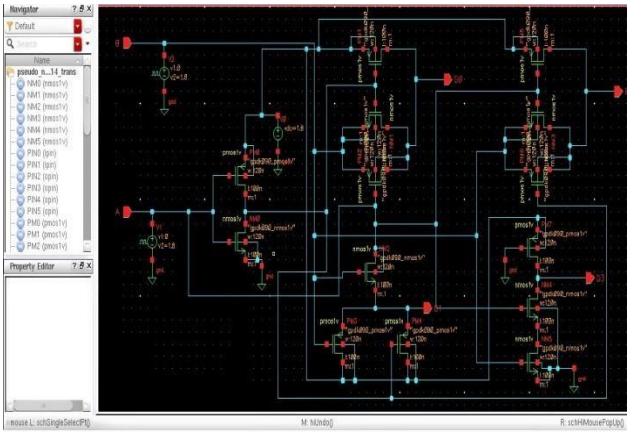

Figure 24. 14-Transistor Pseudo-NMOS Logic for 2:4 Inverting Decoder.

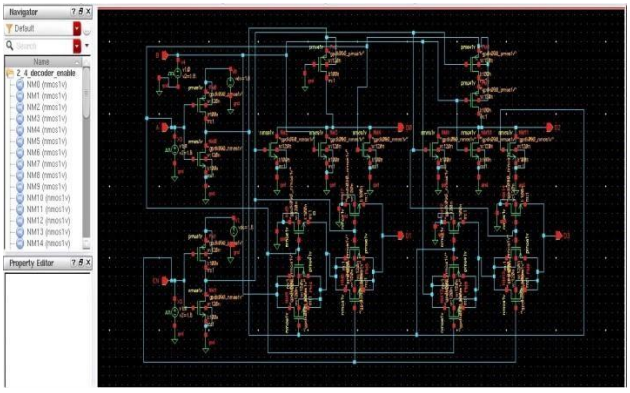

Figure 25. Pseudo NMOS Logic for 2:4 Decoder with Enable.

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Received 25 April 2021: Accepted 08 May 2021.

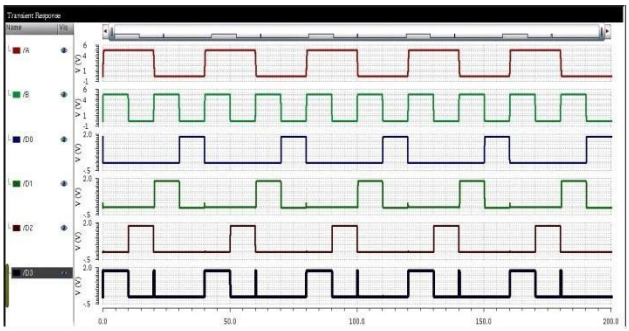

Figure 26. Non-Inverting 2:4 Decoder Output (Transient Response).

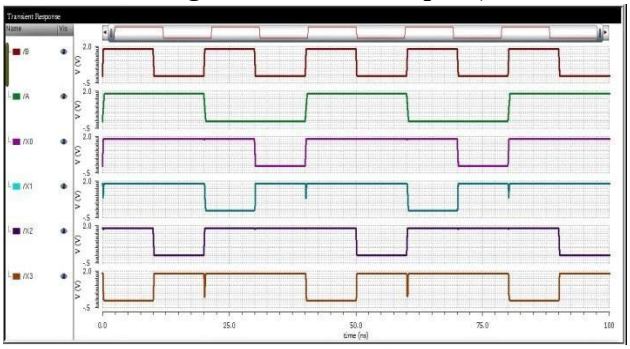

Figure 27. Inverting 2:4 Decoder Output (Transient Response).

The observed power dissipation and delay in the cadence tool are tabulated for 2:4 Decoder with and without enable.

TABLE 5. Calculation Table of 2:4 Decoder without Enable

DESIGN	NO. OF TRANSISTORS	POWER (µW)	DELAY (ρS)
CMOS	20	7.967	111.31
14-T	14	3.093	130.7
15-T	15	3.147	99.72
PROPOSED	14	2.989	70.236
CMOS(I)	20	8.301	113.46
14-T(I)	14	3.876	119.45
15-T(I)	15	3.615	103.898
PROPOSED(I)	14	3.090	77.639

TABLE 6. Calculation Table of 2:4 Decoder with Enable

DESIGN	NO. OF TRANSISTORS	POWER (µW)	DELAY (ρS)
CMOS	20	8.404	226.9
14-T	14	4.867	289.32
15-T	15	5.074	187.93
PROPOSED	14	3.089	149.21

Annals of R.S.C.B., ISSN: 1583-6258, Vol. 25, Issue 5, 2021, Pages. 4637 - 4653

Received 25 April 2021: Accepted 08 May 2021.

CMOS(I)	20	8.219	229.62
14-T(I)	14	4.673	291.21
15-T(I)	15	5.109	190.67
PROPOSED(I)	14	3.178	158.11

CONCLUSION

The static CMOS, TGL, and DVL circuits have been combined to create an effective mixed logic decoder design. The proposed 14-Transistor Pseudo NMOS Logic with low power and high-performance parameters is used to create two new topologies. Standard and inverting 2-4 decoders, as well as decoders either with or without allow feedback applied. in each case. The 2-4 Low Wattage decoders supply more power without as much transistors and are appropriate for a variety of applications where performance and power dissipation are important design considerations, according to simulation results. With fewer transistors, the High-Performance decoders increase both power and delay output and outperform basic CMOS decoders in all parameters. However, the proposed 14-transistor system in every parameter, the pseudo NMOS Logic architecture outperforms the current novel topologies. As a result, the suggested mixed logic decoders use fewer resources and operate better with fewer transistors.

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