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# Implementation of Direct Current Control Strategy For PWM Rectifier Under Unbalanced Input Voltage Circumstances

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***Abstract*****—** This paper proposes an easy and successful current control scheme for an unbalanced supply voltage correction approach in a 3ϕPulse Width Modulation (PWM) rectifier. The voltage unbalance generates input current with higher magnitude and increased Total Harmonic Distortion (THD). The projected direct current controller concurrently minimizes total harmonic distortion and unbalanced components in the supply voltages. The technique is easy to execute and examine well even under extreme non-ideal conditions. The proposed strategy is specifically required to eliminate the second harmonic presented in the DC link. Simulation outcome reveals the best assessment of the suggested controller, despite asymmetry in input voltages. Finally, the results obtained using direct current control is contrasted with the traditional constant frequency method.

**Keywords—**Direct current Control, Fixed Frequency Control, Pulse Width Modulation (PWM), Total Harmonic Distortion (THD).

## I. Introduction

In the recent years, the diffusion of distributed generators into electrical systems has forced the requirement for enhancements in control and design of grid side topologies. The 3ϕ PWM rectifier is a notable methodology has expansively utilized and investigated for this reason [1]. Favorable circumstances of the PWM converter contrasted to other traditional techniques incorporate output voltage control, reduction of low order harmonics, instantaneous power flow inversion ability, and extensive range of power factor control [17].

Unequal working states of the grid- associated sustainable power sources incorporate unbalanced grid voltages (even and uneven voltage dips) and uneven line impedances in [3]. The issues remember a huge twisting for line currents and an massive ripple in the DC intermediate voltage. Additionally,

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unsettling influences in the grid side voltage will build the control complexity by expanding the quantity of changeable targets [18,19].

Six-switch three-phase rectifier has been progressively utilized in the past years leading to the benefits of bi-directional power flow, convenient power factor, sinusoidal line current, and great dc interface voltage guideline capacity [4][5][6]. As indicated by the examination, about 38% of the shortcomings in SSTPR out coming from the power devices break down.

A few papers [7][8] embraced a traditional control strategy dependent on PWM to accomplish elite control of FSTPR. Nonetheless, this strategy can't produce 3ϕ balanced current. Since in an FSTPR, just two-stage line-line modulating waveforms can be produced and the voltage given to all stage are not equivalent due to the capacitor voltage variance at the centre tap.

Current control (CC) of PWM converters is the key subject of present-day power electronics. The primary task of the control plot in the CC–PWM converter is to restrain the controlled currents to pursue the reference signals. Traditional current control strategies can be categorized into non-linear and linear controllers. Linear controllers work with traditional voltage-based PWM modulators in which current mistake reimbursement and voltage adjustment are isolated. The non-linear current control incorporates delta modulation, hysteresis,and on-line optimized regulators [9] [10].

A simple and effective MPC calculation for the current control of a three-stage inverter with symmetrical output voltages and impedances is introduced in [11] [12]. The calculation introduced is not reasonable for the PWM boost rectifier under unequal conditions.

In the presented paper, the $3^{rd}$ rectifier leg is opened, the four-switch three-phase rectifier, which integrates the grid phase with the burden rectifier leg to a midpoint tap of the dc-link capacitors, is a probable solution for fault-tolerant operation, also a current control strategy, are designed to achieve minimum THD operation of the 3ϕ PWM rectifier [13-16]. This paper analyses open-loop and two closed-loop control schemes namely Direct Current Control and Fixed Frequency Modulation of PWM rectifier under various sets of unbalanced input voltage circumstances.

## II. PROPOSED CONFIGURATION

Fig. 1 shows the topology of a 3ϕPWM rectifier where the line voltages can be unbalanced and/or distorted. in which $e_a$, $e_b$, $e_c$ are three-phase power–source voltages; $v_a$, $v_b$, $v_c$ are terminal ac voltages of the PWM rectifier; $i_a$, $i_b$, $i_c$ are 3-phase line currents; This rectifier has two legs with each leg connected to one phase and the third phase connected to the middle tap of two capacitors. The rectifier is allied to the 3ϕ voltage using the LC filter.$S_a$ and $S_b$ are switching states of the converter in each phase leg respectively. $S_k$= 1(k = a, b, c) relates the superior switch of phase k is turned on, and the bottom switch is turned off while $S_k$= 0 illustrates the contradictory meaning. L and r stand for the filter inductance and its equivalent serial resistance (ESR) of each phase. $R_L$ is the load resistance. $C_d$ is the capacitance of the two dc-link capacitors, $u_1$ and $u_2$ are the voltages of the two capacitors, $i_r$ is the rectifier current, $i_L$ is the load current, $id_{c1}$, $id_{c2}$ are the upper and lower capacitor currents, is the total dc-link voltage.

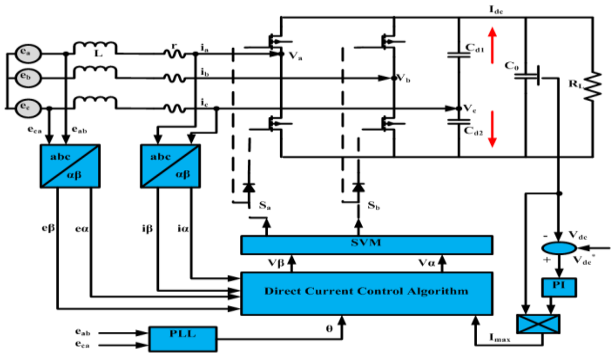


Fig. 1. **Proposed Configuration**

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In this control strategy, the direct current control strategy is intended to calculate the requisite rectifier average voltage vector, once each transition duration, to be applied during the switching period Ts, to void the tracking errors of current vector attributes, $i_\alpha$ and $i_\beta$, at the last part of the transition duration. As revealed in Fig. 1, the power–source voltage vector $V_\alpha$ and $V_\beta$, i/p current vector $i_\alpha$ and $i_\beta$, PI controller output, PLL, and Imax output are utilized as input data variables of the current control algorithm.

The suggested current controller owing to the reduction of output and input harmonics under unbalanced conditions also regulation of power factor at grid terminals. Active power P is obtained at the PI controller output. Whereas, the reactive component Q can be arbitrarily chosen. For power factor unity operation, Q ought to be set to zero. To accomplish steady-state error to be zero for the main current even beneath unbalanced voltage circumstances the input current errors are transformed in a synchronously rotating frame utilizing both negative and positive sequences.

The following assumptions utilized in the expression are:

1. The lossless configuration.
2. The switching functions utilized to characterize switching action of the corresponding unbalanced rectifier
3. Fundamental components of input currents and switching functions are only considered.

The mathematical model of PWM rectifier in abc frame can be expressed by

$$\begin{bmatrix} L\dfrac{di_a}{dt} \\ L\dfrac{di_b}{dt} \\ L\dfrac{di_c}{dt} \\ C\dfrac{dV_{dc}}{dt} \end{bmatrix} = \begin{bmatrix} -r & 0 & 0 & 0 \\ 0 & -r & 0 & 0 \\ 0 & 0 & -r & 0 \\ S_a & S_b & S_c & -1 \end{bmatrix} \begin{bmatrix} i_a \\ i_b \\ i_c \\ i_L \end{bmatrix} + \begin{bmatrix} e_a - v_a \\ e_b - v_b \\ e_c - v_c \\ 0 \end{bmatrix} \tag{1}$$

$$\begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} = \begin{bmatrix} 2/3 & -1/3 & -1/3 \\ -1/3 & 2/3 & -1/3 \\ -1/3 & -1/3 & 2/3 \end{bmatrix} \begin{bmatrix} S_a \\ S_b \\ S_c \end{bmatrix} \tag{2}$$

The abovementioned derivations can be changed into a two-phase stationery (α−β) frame by Clarke's matrix

$$T = \frac{2}{3}\begin{bmatrix} 1 & -1/2 & -1/2 \\ 0 & \sqrt{3}/2 & -\sqrt{3}/2 \end{bmatrix} \tag{3}$$

After Clarke's transformation, the dynamic model of PWM rectifier by neglecting zero-sequence component can be derived as

$$\begin{bmatrix} e_\alpha \\ e_\beta \end{bmatrix} = \begin{bmatrix} L\dfrac{di_\alpha}{dt} \\ L\dfrac{di_\beta}{dt} \end{bmatrix} + \begin{bmatrix} r & 0 \\ 0 & r \end{bmatrix} \begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix} + \begin{bmatrix} v_\alpha \\ v_\beta \end{bmatrix} \tag{4}$$

$$C\frac{dV_{dc}}{dt} = \frac{3}{2}\left(i_\alpha S_\alpha + i_\beta S_\beta\right) - i_L \tag{5}$$

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The two-phase stationary frame voltage and current vectors are given by

$$e_\alpha = E_1 \cos(\omega t + \phi_1) \qquad e_\beta = E_2 \cos(\omega t + \phi_2) \tag{6}$$

$$e'_\alpha = E_1 \sin(\omega t + \phi_1) \qquad e'_\beta = E_1 \sin(\omega t + \phi_1) \tag{7}$$

$$i_\alpha = I_1 \cos(\omega t + \phi_3)$$

$$I_\beta = I_2 \cos(\omega t + \phi_4) \tag{8}$$

$$i'_\alpha = I_1 \sin(\omega t + \phi_3) \qquad I'_\beta = I_2 \sin(\omega t + \phi_4) \tag{9}$$

$$V_\alpha = V_1 \cos(\omega t + \phi_5) \qquad V_\beta = V_2 \cos(\omega t + \phi_6) \tag{10}$$

$$V'_\alpha = V_1 \sin(\omega t + \phi_5) \qquad V'_\beta = V_2 \sin(\omega t + \phi_6) \tag{11}$$

The instantaneous reactive and active powers at the input terminal are defined as

$$P_{in} = \frac{3}{2}\left(e_\alpha i_\alpha + e_\beta i_\beta\right) \tag{12}$$

$$q_{in} = \frac{3}{2}\left(e'_\alpha i_\alpha + e'_\beta i_\beta\right) \tag{13}$$

Where $p_{in}$ and $p_{out}$ are the instantaneous powers at the input and rectifier terminal respectively. If the devices used in the proposed circuit is ideal, the instantaneous power consumed by the input filter is equal to the difference among i/p and o/p power ($P_{in}$-$P_{out}$), whereas, output power ($P_{out}$) is equivalent to the power delivered to the dc bus capacitor and the load. Similarly, the instantaneous reactive and active powers at the output terminal or the pole of the rectifier are defined as

$$P_{out} = \frac{3}{2}\left(v_\alpha i_\alpha + v_\beta i_\beta\right) \tag{14}$$

$$q_{out} = \frac{3}{2}\left(v_\alpha i_\alpha + v_\beta i_\beta\right) \tag{15}$$

## III. Results and Discussion

The working of the 3ϕ PWM boost-type rectifier under a severe unbalanced and distorted operating situation has been simulated in MATLAB Simulink by utilizing the simpower system toolbox. The simulation parameters appear in table I. Three different cases of three-phase balanced and unbalanced voltage have been chosen to confirm the feasibility of the projected current control strategy with the conventional fixed frequency control method. Each case's output voltage, supply current, and harmonic distortion is analyzed and compared. From the analysis, it is displayed that the voltage output still constant for all the unbalanced and balanced voltage circumstances. Figure 2 demonstrates that the 380 V is obtained from a conventional method and 400 V is obtained from the proposed current control algorithm. From the examination made it is concluded that the Direct Current control has a minimum THD of 2.31 % than that of Fixed Frequency Modulation method which has THD of 4.34%.

TABLE I. **Simulation Parameters**

| | |
|---|---|
| Dc Bus Capacitor | C=1100 µF |
| Filter Inductor | 1 mH |
| Dc Bus voltage | Vdc=300 V |
| Load resistance | 100 Ω |

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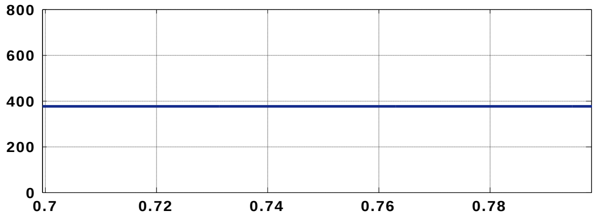
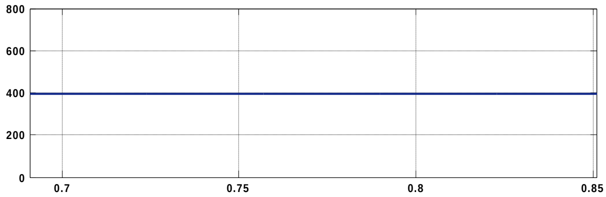
| | |
|---|---|
| Switching Frequency | 5 kHz |
| Sampling Frequency | 10 kHz |
| Source Voltage(Line-to-Line, RMS) | 160 V/50 HZ |



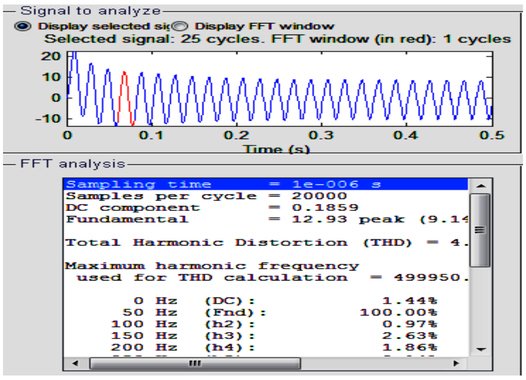

(a)



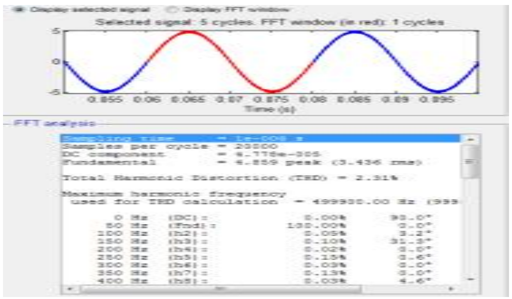

(b)

Fig. 2. **Output voltage (a) Conventional controller (b) Proposed controller**

*A. Case 1: Balanced Supply Voltage [$V_a$=$V_b$=$V_c$=200]*




**(a) THD observed is 4.34%**



**(b) THD observed is 2.31%**

Fig. 3. **Supply current and THD (a) Conventional controller (b) Proposed controller**

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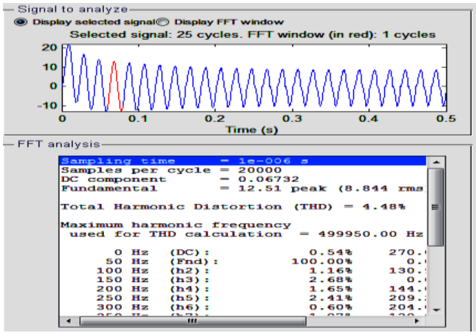
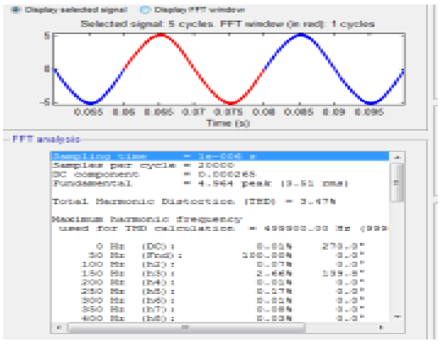
*B. Case 2: 10% Unbalanced Supply Voltage [$V_a$=200, $V_b$=220 and $V_c$=240]*




**(a) THD observed is 4.51%**

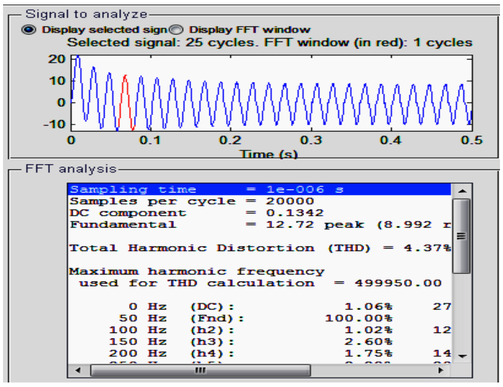



**(b) THD observed is 3.47%**

Fig. 4. **Supply current and THD (a) Conventional controller (b) Proposed controller**

Fig. 3 illustrates the simulation waveforms under balanced operating circumstances using case 1 to generate the references. The current waveforms are sinusoidal through unbalanced while the output DC voltage is stable with minimum ripple. Fig. 4 and Fig. 5 displays the simulation waveforms under 10% and 5% unbalanced operating condition using case 2 and case 3 to generate the references. The current waveforms are sinusoidal through unbalanced while the output DC voltage is stable with minimum ripple.

*C. Case 3: 10% Unbalanced Supply Voltage [$V_a$=210, $V_b$=220 and $V_c$=230]*




**(a) THD observed is 4.38%**

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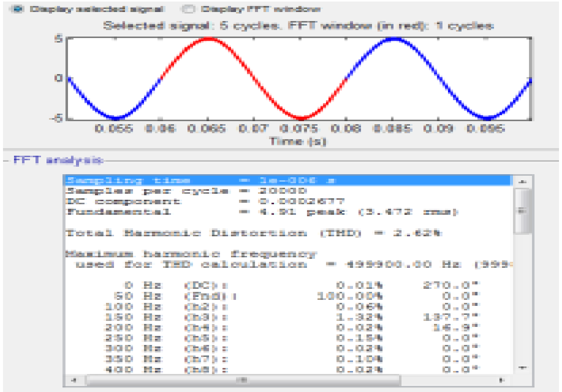

**(b) THD observed is 2.62%**

Fig. 5. **Supply current and THD (a) Conventional controller (b) Proposed controller**

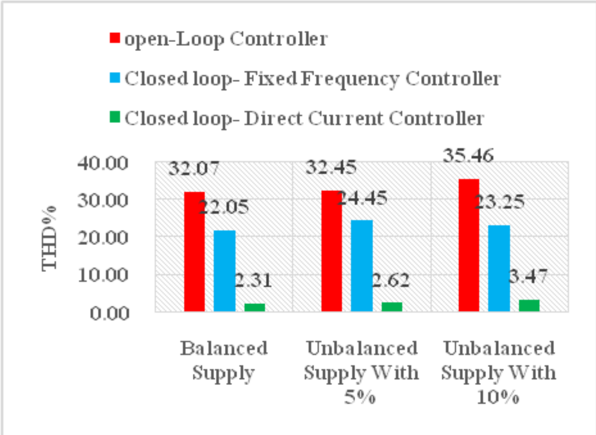


Fig. 6. **Comparison analysis**

Fig.6 shows the comparative analysis of the proposed direct-current controller with open-loop controller and closed-loop fixed-frequency controller and observed that the projected controller has minimum THD compared to other existing methods under all balanced and unbalanced supply voltage circumstances.

## IV. CONCLUSIONS

In this paper, the analysis of PWM Rectifier under Unbalanced Input Voltage Conditions has been presented. The analysis incorporates the harmonic assessment of the input current waveform. It has been shown that the input voltage unbalance generates input current with increased Total Harmonic distortion(THD). Also the magnitude of input current increases. To conquer the mentioned issues two types of control schemes namely Direct Current Control and Fixed Frequency Modulation. From the analysis made it is evident that the Direct Current control is much better than that of Fixed Frequency Modulation

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