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Design and Analysis of Dynamic Comparator based on Cross Coupled Inverters for Low Power and High-Speed ADC Applications

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Abstract:
Now a days CMOS dynamic comparator mostly used for the analog to digital (A/D) conversion applications, because of high speediness and power minimization, low immune to noise characteristics. The proposed topology described in this project i.e., dynamic comparator based on cross coupled differential pairs inverters as the latching stage, which affords a positive feedback and gives extraordinary improvement switchable current sources. It will work with less static power consumption, higher speediness and minimize the area. The conventional latching level has two transistors with zero voltage in between gate to sources, which minimize the total effective trans conductance of latching level. In this paper dynamic comparators using a cross-coupled inverters, decrease the power consumption also very much useful for high-speed Analog to Digital conversion application. The dynamic comparator circuit designed with 0.13 μm CMOS technology by using Mentor Graphics Tool for simulating transient response and dc response results. Layout of the recommended cross coupled dynamic comparator has been done in Mentor graphics EDA tool and finally compared the schematic and layout using layout vs schematic (LVS).

Index Terms: Cross-coupled dynamic comparator, high speed, low area, low offset voltage, power minimization

1. Introduction

The analog to digital conversion most probability have used crucial module is latch-based dynamic comparator [1-5], high speed digital I/O circuits [6], memory sensing amplifier [7]. To get high gain we have used positive feedback in dynamic comparator associating through a static comparator. The dynamic comparator has high speed and static power is very truncated [8-11] the dynamic comparator input transistor immediately stacks through the cross-coupled dynamic comparator circuit. In voltage control ring oscillator lesser power consumption and wide range of frequency application [9-13]. In Double gate MOSFET based voltage control oscillator (VCO) used for low frequency applications [18]. Delay locked loop is a major block is synchronous integrated circuit which is great speed circuit. Which is widely used in phase frequency detector[14-16].Single stage amplifier or differential amplifier which is improve the strength of weak signal by the output section [17].In cross-coupled dynamic comparator has large voltage headroom [19] and also suffer with several kickback noise. Moreover, the capacitive paths from output nodes to built-in nodes and also main difficult tradeoff among power utilization and speed. Introduced several technique low power utilizations and less voltages dynamic comparators with the charge-steering technique [20] and supply increasing methods as well as increase the speediness and less power applications[21-23] .While we have using dual stage, dynamic comparators containing fully dynamic pre amplifier as input level this is separating from latching level then we have providing the fewer stacking. It is useful for low-voltage operations and also reduce the

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bribe, noise we have offering extra protecting among input side and output side both are enable which be governed by on the optimization of the input level it is disturbs the offset and latching level which is mainly affects the speed. After many modifications to achieve quicker spee**d** and lesser power consumption. In preamplifier stage of dynamic comparator strengthen the regeneration which is reduced delay [24,25]. In the pre amplifier stage positive feedback is used in the of cross coupled dynamic comparator and also dynamic comparator agonize with high inducement noise [27]. The latch is activating with a calculated delay to decrease power utilization mostly it is very difficult designing the requirements. Actually, it takes a large necessary area and greater kickback noise [26]. In preamplifier stage we have improve gain and also positive feedback given to the preamplifier stage and special clocking technique is used in cross coupled dynamic comparator amplification stage [28].The working principal of dynamic comparator to compare the analog voltages one is input voltage another one is reference analog voltage and the output is becomes binary digits either 0 or 1 based on comparation [31]

The paper is arranged as follows. In the section II discuss the basic dynamic comparator block diagram and then section III discuss the conventional two-stage comparator operation and delay analysis. In the section IV we have discuss the proposed comparator and the designing consideration. In the section V simulation as well as result will be discuss and section VI concluded this paper

2. Basic block diagram of dynamic comparator

Figure1 shows basic comparator block diagram. Dynamic comparator has one of major block in the analog-digital conversion applications. Most of the analog to digital conversions comparators are widely used. The block diagram contains preamplifier stage and latching stage. There are many types of comparators, but dynamic comparator frequently used and designed for low power applications. In the pre-Amplifier stage increases gain by using the positive feedback and improve speed of operation by using the latching stage. Mostly cross-coupled dynamic comparator used in various type of applications.

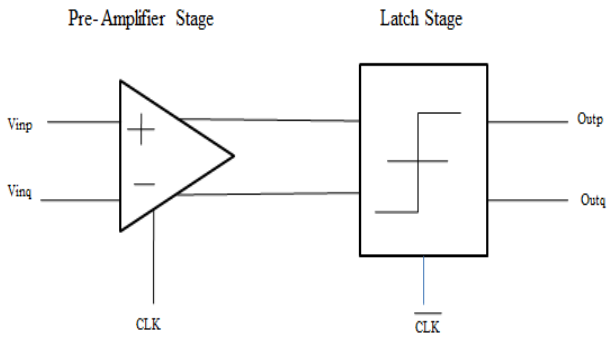

Fig.1. Basic Comparator Block Diagram

3. Two-stage conventional dynamic comparator

The two-stage conventional dynamic comparator contains preamplifier stage and latching stage. In the preamplifier stage reducing offset voltage at the input and circuit performance of speed operation is depended on the latch circuit. In the conventional two stage dynamic

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comparator amplifier stage providing strong positive feedback which gives high dc gain and latching stage provides high speed

The circuit operation as shown in Figure 2 while clock is connected to the ground CLK=GND, M9 as well as M10 both are on condition, by the time M1 in addition to M13 both the transistors are off mode. The joints Cp along with Cq both are charged up to VDD, then the connections OUTp as well as OUTq to discharged towards ground via M7 and M8. The evaluation phase CLK= V_{DD}, M1 as well as M13 going to on mode, along with M9 and M10 both the transistors off mode. The joints Cp along with Cq starts to discharge depending on input voltages. The cross coupled dynamic comparators have several advantages i.e reduced voltage operation and less kick back noise. The main disadvantage of conventional two-stage comparator clock needs high precision timing since the latch level takes to restore the differential input voltage coming from input level at very small time. Instantly we have replacing the invertor which output node is connected towards the input node of M1 transistor the clock signal drives stronger load in order to push leading transistor M1 in a lowest probable delay. So in this drawback we can go to the cross-coupled conventional dynamic comparator which decrease the delay and also gives low immune to noise. The conventional dynamic comparator operates two different modes of operations that is reset mode clk=0. Similarly comparation mode clk= V_{DD} these two modes of operations very important.

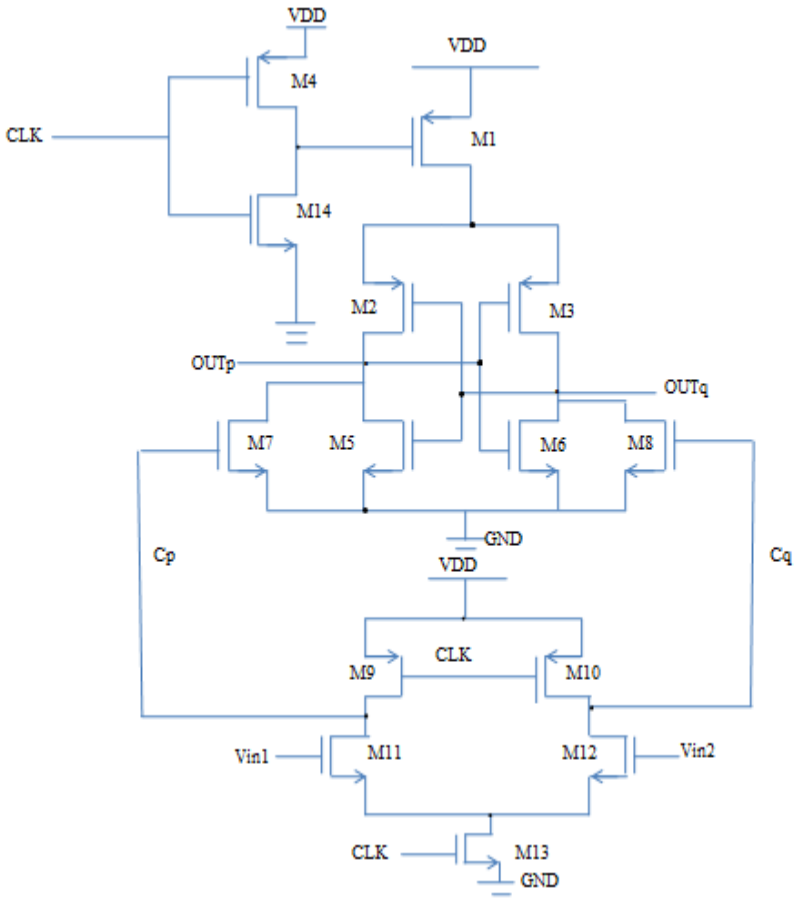

Fig.2. Schematic of the conventional two stage comparator

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4. Proposed cross-coupled dynamic comparator Circuit

4.1 Description of circuit

The operation of cross-coupled dynamic comparator shown in Fig.3.while phase will be reset at what time CLK=GND, the nodes Bp along with Bq both are charging towards VDD, and then M7, M1 and M8 these are on mode condition, and M3 as well as M4 both are off mode condition. The protuberances are Bp as well as Bq both are discharge towards ground through transistor M7 and M8, the OUTp as well as OUTq both nodes charged to VDD through transistor M1 and M2. In reset phase two transistor in strong inversion section in additional two transistor in cut-off section, all cross-coupled transisrorsM1, M2, M5 and M6 in re-forming construction are biased in strong inversion section. In regenerative stage gives higher effective trans conductance compare to the conventional normal dynamic comparator. In cross-coupled dynamic comparator gives shorter metastable period and also it is reduce the energy consumption. Invertor based cross-coupled dynamic comparator to improve speed of operation and effect of trans conductance.

At a time period t = t_0 discharged output from V_{DD} then the transistors M_{1-2} and M_{5-6} goes to triode region then trans conductance of latching stage can be expressed as

$$g_{m,n} = \mu_n C_{ox}(w/L)_n V_{dsn} \quad (1)$$

$$g_{m,p} = \mu_p C_{ox}(w/L)_p \ |V_{dsp}| \quad (2)$$

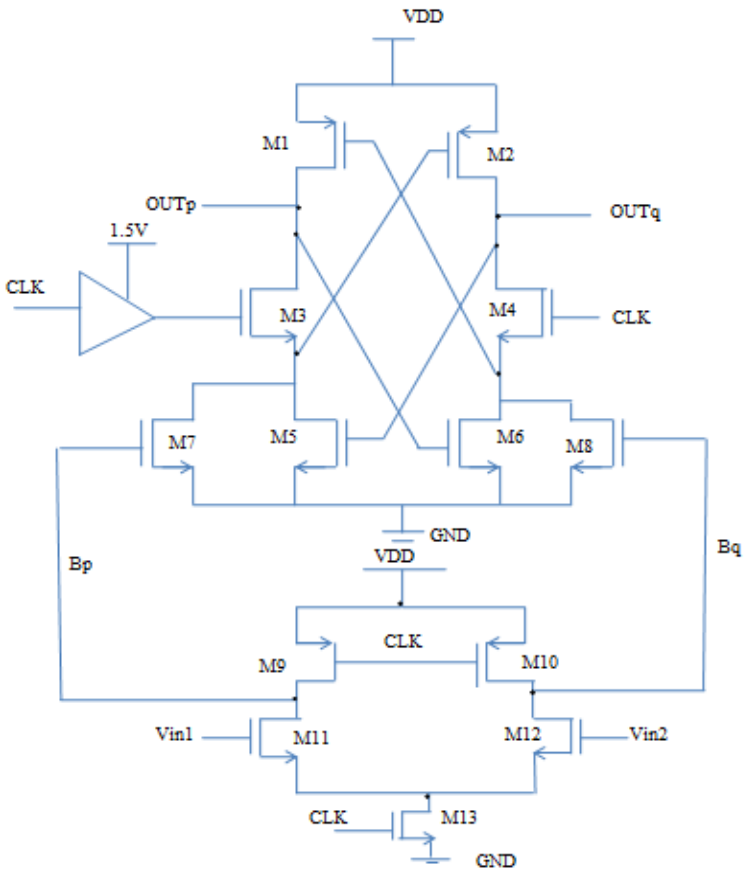

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Fig.3. Schematic diagram of proposed dynamic with two stages comparator

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Where eqations1 &2 represents transconductance of N &P MOS transistors then the effective transconductance expressed as

$$g_{m,eff} = g_{m,n} + g_{m,p} \quad (3)$$

$$g_{m,eff} = \mu_n C_{ox}(w/L)_n V_{dsn} + \mu_p C_{ox}(w/L)_p \ |V_{dsp}| \quad (4)$$

After some time clk signal will be increases to V_{DD} then the transistors M3 and M4 are turned on these two transistors are P-MOS transistors. It will be goes to saturation region. The trans conductance of P-MOS transistors saturation region can be expressed as

$$g_{m,eff} = \mu_p C_{ox}(w/L)_p \ (|V_{dsp}| - V_{thp}) \quad (5)$$

Whereas the transconductance of cross-coupled invertor based dynamic comparator improve speed at latching stage compare to the normal dynamic comparator and also it will be lower energy consumption. In the reset phase some normal dynamic comparators two transistors goes to the strong inversions region two transistors goes to cut-off region. In the comparison phase dynamic comparator comparing two voltage levels one is input analog voltage another one is reference voltage signal. The cross-coupled invertor contain the buffer stage which leads to the reduced the power consumption .The cross-couple dynamic comparator time delay can defined as time taken output to reaches the 0.5 V_{DD} expression can be expressed as

$$t_{delay} = t_{op} + t_0 + t_{latch} \quad (6)$$

The transconductance of M1 and M2 nearly equal to the total delay of of transconductance of latching stage and t_0 can be expressed as

$$t_0 = \frac{V_{th\,n} C_L}{I_p} = \frac{V_{th\,n} C_L . 2\mu_p C_{ox}(w/L)_p}{g_{m,eff}{}^2} \quad (7)$$

Where $\mu_p$mobility of the holes, Load capacitance of the output is C_L ,Gate oxide capacitance C_{ox}, $V_{th\,n}$ is threshold voltage. g_m is trans conductance of M1 transistor, W_P and L_P are channel length and width of transistor M1.

The latch time of cross-coupled dynamic comparator will be defined as change of voltage at output reaches to 0.5$V_{DD}$the latch time will be expressed as

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$$t_{latch} = \frac{C_L}{g_{m,eff}} \ln \frac{\Delta V_{OUT}}{\Delta V_0} = \frac{C_L}{g_{m,eff}} \ln \frac{0.5V_{DD}}{\Delta V_0} \quad (8)$$

Where ΔV_{OUT} change in the output voltage and ΔV_0 is change in the initial output voltage at the time period t = t_0

The cross-coupled dynamic comparator total delay can be expressed as

$$t_{delay} = \frac{V_{th\,n} C_L . 2\mu_p C_{ox} (w/L)_p}{{g_{m,eff}}^2} + \frac{C_L}{g_{m,eff}} \ln \frac{0.5V_{DD}}{\Delta V_0} \quad (9)$$

While using invertor based cross-coupled dynamic comparator reduced the delay in the comparing phase. The lower regeneration no impact on trans conductance of NMOS.Only impact on trans conductance of PMOS.

4.2 Design Considerations

Several issues are raised while we have design circuits. Considering will be taken while we have designing cross-coupled dynamic comparators. Generally distinctive part of shape customized cross-coupled latch level and knobs M3 and M4. In comparison phase M3 and M4 are turned on then discharge path of output nodes from drain to source voltage of these adjustment should be reduced. The parasitic capacitance of M3 and M4 is a amount of load capacitance. The controller signal CLK1 is a improved as well as delay signal which is generate CLK. When the dissimilar width are providing the transistors M3-4 because reduce time delay and power utilization.

Table 1 Proposed dynamic comparators transistor sizes

Transistor number	Size of transistor (μm)
M1-2	2/0.13
M3-4	1/0.13
M5-6	0.5/0.13
M7-8	2/0.13
M9-10	1.8/0.13
M11-12	4/0.13
M13	0.44/0.13

5.1 DC Analysis:

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Figure 4 shows the DC Analysis graph of the conventional comparator. Input voltage is taken as 1 V and swept from -1V to +1V. Reference Voltage is put as 2V. From the graph we can conclude that the comparator is working fine

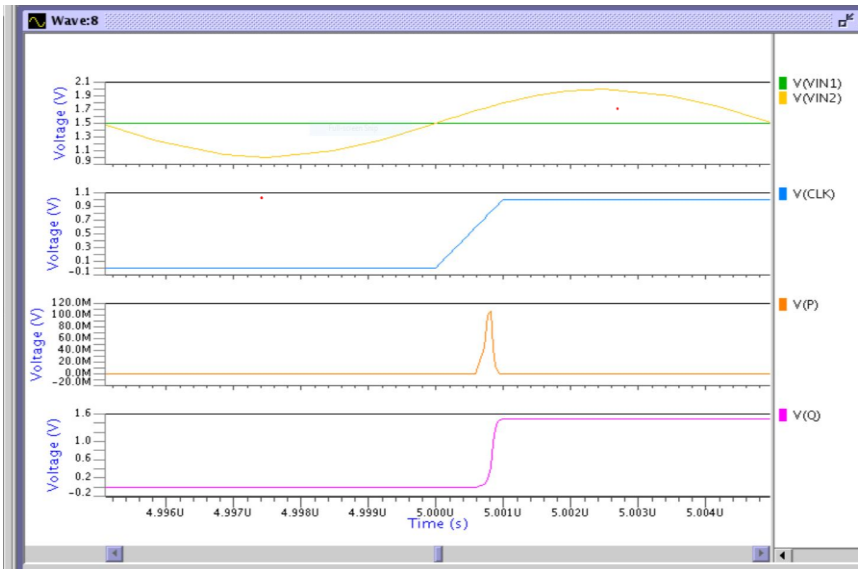

Fig.4. DC response of the Conventional Dynamic Comparator

5.2 Transient Analysis:

Figure 5 shows the transient analysis of the conventional dynamic comparator circuit. From this analysis we can about that yield of v(p) node in latch stage is affected by noise and fluctuating with the clock transition as that was in the existing comparator. For the transient analysis we have taken pulsate voltage source as Input stage and a dc voltage source as reference node.

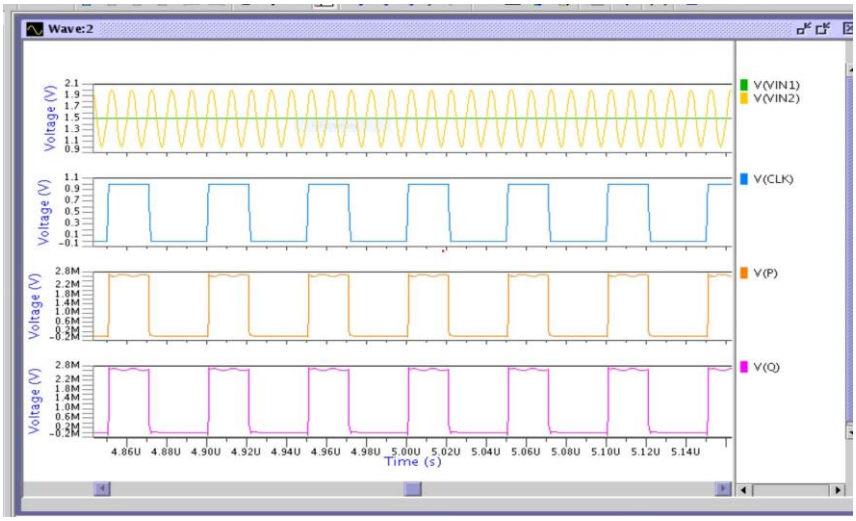

Fig.5. Transient Response of Conventional Dynamic Comparator

5.3 DC Analysis:

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Figure 4 shows the DC Analysis graph of the proposed cross-coupled dynamic comparator circuit. Input voltage is taken as 1.5 V and swept from -1.5V to +1.5V. Reference Voltage is put as 2V. From the graph we can conclude that the comparator is working fine

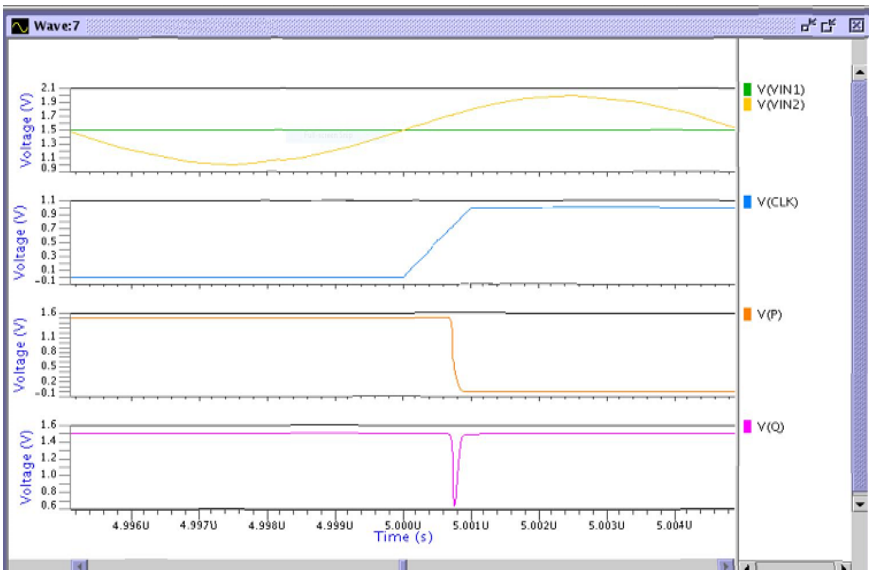

Fig.6. Dc response of the proposed cross-coupled dynamic comparator

5.4 Transient Analysis:

Figure 5 shows the transient analysis of the proposed cross-coupled dynamic comparator circuit. From this analysis we can about that the output of v(p) node in latch stage is affected by noise and fluctuating with the clock transition as that was in the existing comparator. For the transient analysis we have taken pulse voltage source as Input stage and a dc voltage source as reference node.

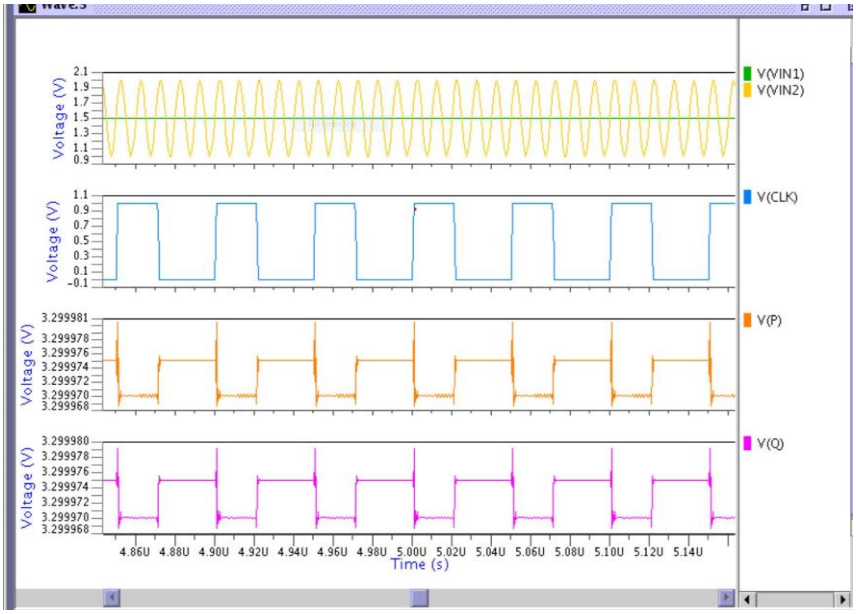

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Fig.7. Transient response of proposed cross-coupled dynamic comparator

In Figure 6 and Figure 7 Delay comparisons and Energy comparison of proposed dynamic comparator comparators and conventional dynamic comparator.

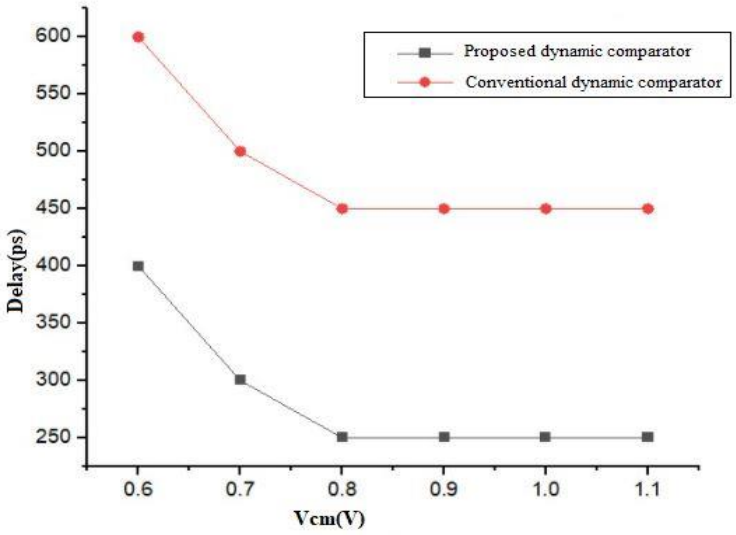

Fig.6. Simulated delay comparisons of conventional and cross-coupled dynamic comparators

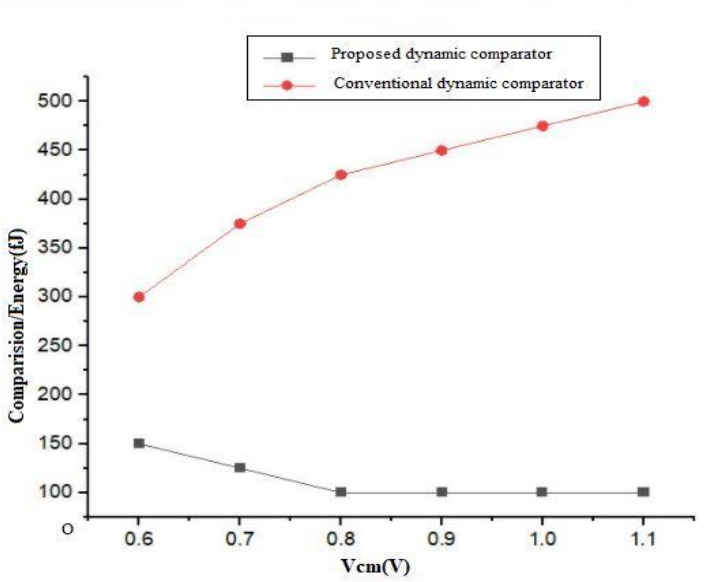

Fig.7. Simulated energy per comparison

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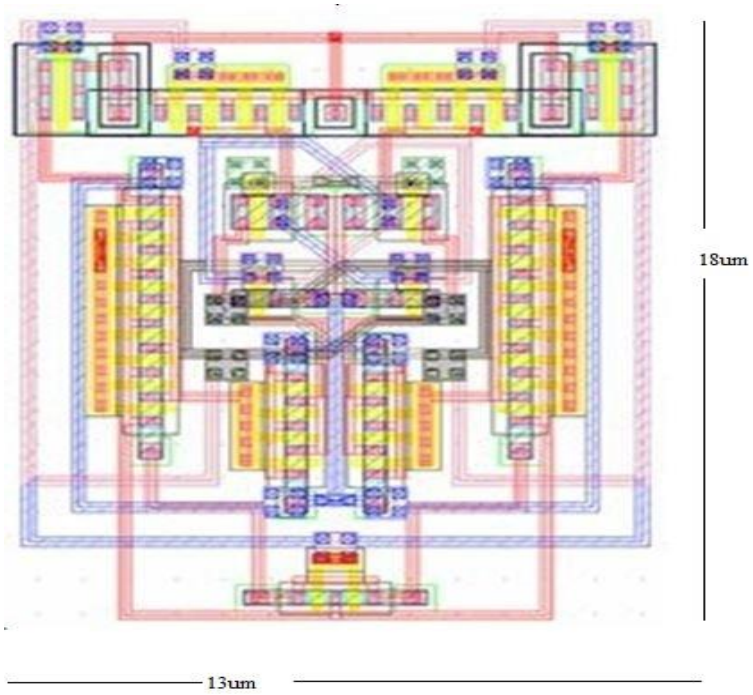

Fig.10. Proposed cross-coupled dynamic two-stage comparator layout

Table 2: Result summary before layout

COMPARATORS	Transistor Count	Offset Voltage (mv)	Power Dissipation (µw)	Delay (ns)	Speed (GHz)	Slew Rate (V/ns)
Preamplifier Based Comparator [11]	22	64.35	83.45	0.393	2.54	21.23
Latch Type Voltage Sense Amplifier [2]	19	339.6	14.84	1.247	0.802	11.08
Double Tail Latch Type Voltage SA[3]	22	259.8	127.9	1.745	0.573	39.85
Dynamic Comparator without Calibration [4]	23	300.1	105.33	0.61	1.639	3.09
Double Tail Dual Rail Dynamic Latched Comp.[5]	27	300	57.37	1.49	0.671	10.77
Proposed dynamic Comparator	17	7.25	75.3	0.38	1.5	10.26

Table 3: Summary of Post Layout Simulation Results

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COMPARATORS	Power Dissipation (µw)	Delay (ns)	Speed (GHz)	Slew Rate (V/ns)	Area (μs^2)
Latch Type Voltage Sense Amplifier[2]	16	1.35	0.735	18.27	84.28
Double Tail Latch Type Voltage SA[3]	145.07	2.52	0.390	2.16	86.24
Dynamic Comparator without Calibration[4]	110	1.95	0.510	16.37	124.23
Double Tail Dual Rail Dynamic Latched Comp.[5]	65	2.15	0.460	11.07	110.24
Conventional dynamic comparator[31]	123.3	0.76	1.25	7.62	543
Proposed dynamic Comparator	82.25	0.42	1.5	6.95	234.42

6. Conclusion

The proposed cross-coupled dynamic comparator has latching stage and preamplifier stage. In latching stage provided strong positive feedback and also reduced static power consumption. In preamplifier stage improves gain and reduced the noise. The cross-coupled dynamic comparator has majorly classified two phases they are reset phase and comparison phase. In reset phase latching circuit is biased in strong inversion region which leads to improving trans-conductance of the latch. In comparison phase to reduce delay as well as power consumption. The layout for the designed circuit is done for fulfillment of simulated results at CMOS 130 nm technology which is occupied less area as compared to existing one

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