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Design and ASIC Implementation of Efficient 8-bit Integer Division Algorithms

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Abstract— Many algorithms are developed for implementing division in hardware. This paper describes the efficient 8-bit integer division algorithms. The 8-bit division algorithms are intended and enforced Verilog code in activity model. Then the division algorithms are synthesized and enforced on ASIC Implementation. A division could be purposefully a slice of the arithmetic and logic unit and division is the one foremost difficult operation among all the fundamental arithmetic operations. In this paper we have designed 8-bit division algorithm for signed and unsigned numbers that performs specific division operations. When the results are analyzed, comparison of performance parameters (like speed, area, delay and power consumption) are optimized. Verilog Hardware Description Language (HDL) is used to verify the functionality of the considered algorithms and synthesized using cadence tool and the layout has beengenerated. Nc-launchhasbeenusedforsimulation,genus for the synthesized design and innovus is used for physical design. Compared to all proposed algorithms the restoring unsigned division algorithm consumes the total power of 0.8107 mW and minimum netlist of213.

Keywords—Division Algorithms, restoring and non-restoring division algorithms, Verilog, ASCII.

I. INTRODUCTION

Since its inception, computers have evolved rapidly. The primary function of computers is to perform mathematical operations to execute programs and applications. Addition, multiplication and division are the three basic arithmetic operations performed by computers. Separation, in addition and multiplication, is a less wasteful operation. Computers, on the other hand, lose capacity if the partition is ignored. Device based partitioning algorithms can be divided into three categories: number iteration, functional iteration, and table-based policies. Each approach has its own set of advantages, but the number of iterative sections is the most commonly used algorithm for division and origin in most floating-point units, because it is straightforward and less difficult. For no repetitive partitioning, recovery and non-retraction algorithms are prototypes. Subtracting the divider from the dividend rather than the divisor is the same division before the remaining amount is less than the divisor.The number of subtractions is that the quotient, and thus the number left is that the rest, this process is extremely time consuming.

Barrier is an important component of equipment and has long been used in advanced signal processing units (DSPs). In high-precision advanced and fast processing (DSP) science processing units, the diaphragm is attached to the indispensable and simple nursing unit. Unlike other scientific processes, this section is characterized by systematic and precise processes that lead to the use of complex devices. Integer division is called integer division.Dividing the whole by two numbers is a number grinding process.

In restoring division, subtraction carryon until there is change in the sign of the fragmented remainder.The modificationpurpose is instantaneous addition of the divisor and a consequent decrement of the accumulating quotient, ahead the proper shift. In non-restoring division, the change in the sign bit causes a shift consequently in one or more additions up to the sign changes back. The design of fast dividers is an dominant issue in high-speed computing because division accounts for a significant fraction of the entire arithmeticoperation.

ASIC: In a lath sense, an integrated circuit customized for the specific applications or end use rather than using it for the standardized purpose is usually defines the ASIC (Application Specific Integrated Circuits). Figure 1 shows the timber of ASIC. Due to the application specific custom nature of the ASICs,

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they usuallycompress more functionality at the similar time delay which is much smaller in size, consumed with less power and dissipating lesser heat whencompared to a standard IC solution.

Figure 1: A timber of ASIC (Application-Specific Integrated Circuit)chips

ASICs are absolutely different from fartherstandardized ICs like Microprocessors or storage devices as these are constructed which can be utilized in the wide range of applications. In contrast, an ASIC can only be used in the application it was specifically designed to run.

II. DIVISIONALGORITHM

Division algorithm repeatedly subtracts the divisor (multiplied by one or zero) from acceptable bits of the dividend. Therefore, subtraction and shift operations are the two primary operations to implement the division algorithmic rule. After every subtraction, the divisor (multiplied by one or zero) is/are shifted to the proper by one bit relative to the dividend. For the circuit implementation, dividend is shifted left instead of shifting the divisor. Integer division in hardware isaccomplished and consummated through subtraction and shifting of digits specifically like typical longhand division within the crudest technique, whereas higher ways use algorithms that calculate the result a slew of faster and in countable steps.

The division algorithms repeatedly subtract the divisor from acceptable bits of the dividend. Therefore, subtraction and shift operations are the two primary operations to implement the division algorithms.The code written within the software is implemented using ASIC where the physical design of the proposed algorithms has been generated with optimized power, area, delay and the netlist. During the implementation

Consider the example to division operation using restoring algorithm for unsigned number as shown in Table 1 below where the dividend is taken as 11 that is 1011, divisor is 3 i.e.,0101 and number of bits are 4. When the count or the number of bits value is 0, the reminder is stored with the of A i.e., 00010 and Quotient is stored with the value of Q i.e., 0011.

dividend is shifted left rather than divisor. Table I: Example of restoring division for unsigned numbers

III. RESTORING DIVISION ALGORITHMS FOR UNSIGNED AND SIGNED INTEGER NUMBERS

In the restoring division method, the width limit comparisons used to obtain a new quote number are a prominent feature of the quote recovery process. In this algorithm the denominator is changed and removed from the divisor. The policy fails at this bit position, and if the divisor is removed and a negative result is obtained for each bit position relative to the divisor, zero is assigned to its equal position. The divisor is added back (restored) to the results of the division operation, then the subsequent highest little bit of the dividend is shifted into the left bit position of the result. The quotient increases from left to right as each part of the dividend is moved from right to left. The partition ends after n moves, where n is the sum of the bits in the partition. Figure 2 describes the complete flowchart for retrieving division algorithms for unsigned integers.

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N	A	Q	Operations
4	00000	1011	Initialization
	00001	011_	Shift Left AQ
	11110	011_	A=A-M
3	00001	0110	A[n]=, Q[0]=0, A=A+M ,n=n-1
	00010	110_	SL AQ
	11111	110_	A=A-M
2	00010	1100	A[n]=1, Q[0]=0, A=A+M ,n=n-1
	00101	100_	SL AQ
	00010	100_	A=A-M
1	00010	1001	A[n]=0, Q[0]=1, n=n-1
	00101	001_	SL AQ
	00010	001_	A=A-M
0	00010	0011	A[n]=0, Q[0]=1, n=n-1

The algorithms are coded using FSM Logic which is shown in the figure 3.

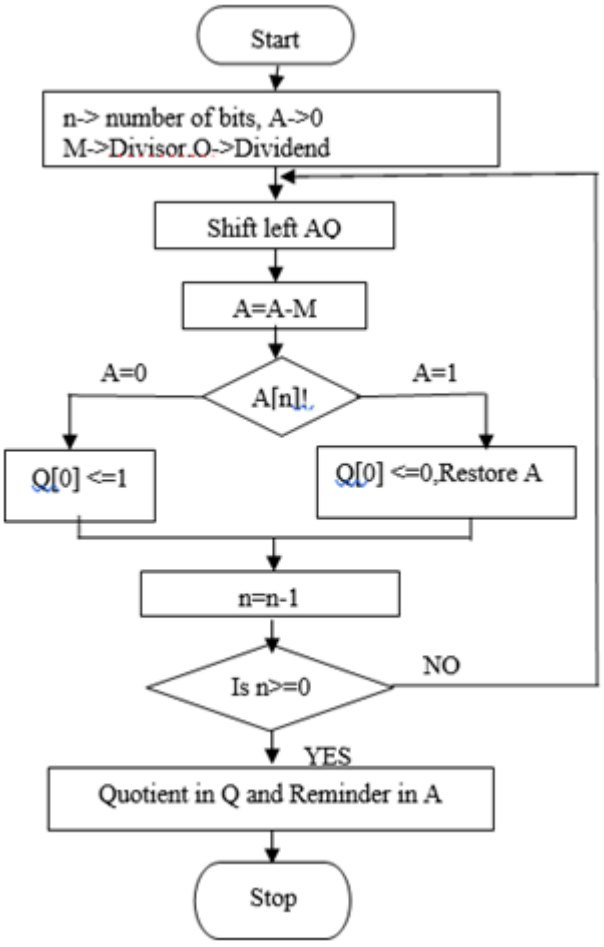

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Figure2:Flowchartforrestoringdivisionalgorithmsfor unsigned integernumbers

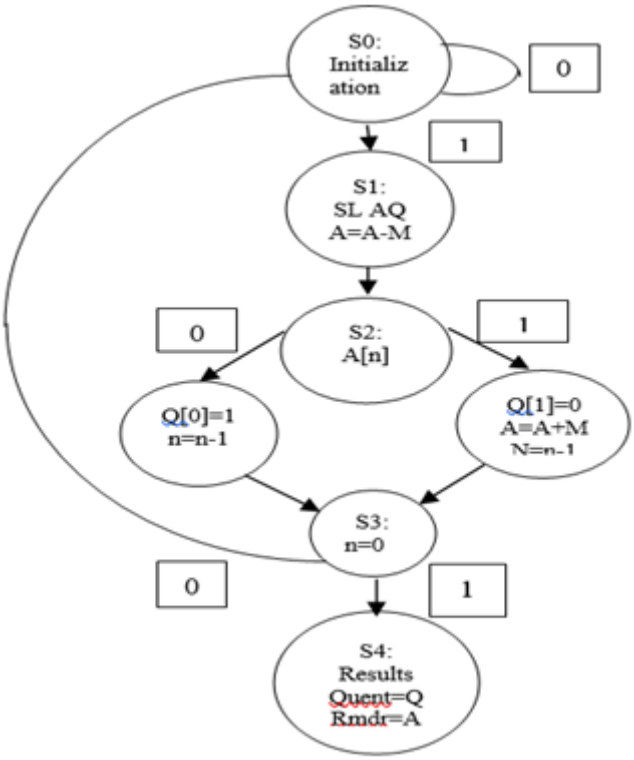

Figure 3: FSM Logic for the restoringalgorithm for unsigned integer

The Algorithm for restoring division for signed integer are as follows:
Step 1: First, the records are started with the corresponding values (A1N-1) = 0, A2 [N-1] = dvnd, B [N-1] = dvsr, Q [2N-1] = 0 and count = 2N)
Step 2: The XOR operation then takes place from A2 and B for [N-1], and the value is stored in "Record".
Step 3: If the bit of A2 is [N-1] 1, then run compliment 2 for A2 and add “1”, otherwise the left move removes B from A1A2 and A1, stores the “T” register and MSB is stored for Q By bit value [N-1] for "T".
Step 4: Check the bit [N-1] if B is 1, fill 2 to B and add “1”, then move A1A2 to the left, subtract B from A1 and store the “T” record, then Q Is stored with the bit [N-1] value for MSB "T".
Step 5: Check the most important bit in Q, if it is a store, the 'T' value in A1 will reduce the count value, if the count value becomes zero, we will exit the loop, or repeat
Step 6: Step 4 after 6, after the count value is zero, Check the MSB for "Register", if it is "1" then add 2 for Q and "1", otherwise the record Q will contain codeine and A will have the rest.
Similarly, as in the above considered algorithm, the procedure is carried out in the upcoming considered algorithms where the coding is designed using FSM logic, verified using Verilog, emulated with the Cadence RTL compiler, and implemented in Cadence encounter digital execution tool.
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IV NON-RESTORING DIVISION ALGORITHMS FORUNSIGNED AND SIGNED INTEGER NUMBERS

If -1, 1 which are the signed binary numbers is considered, then they are pre-owned to describe the content bits, then the non-retrospective division approach has built-in support for the signed number systems. Parameters must be submitted in supplementary form 2 to submit the Number Section (NRTS). During execution, the content bits -1 and 1 are encoded as 0 and 1, respectively. Using the standard format, the signed binary score, i.e., Q, is translated as 2 'binary complement. In the non-refundable process for unsigned numbers, the contents in traditional binary number charts are selected as 0 1. Figure 4 shows the complete flow chart of the undetected division algorithm for the signed numbers.

For unsigned numbers, irreversible partition algorithm:

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Step 1: Format the records with the appropriate values (Q = dividend, M = divisor, A = 0, n = number of bits in the dividend).
Step 2: If the most important bit of A is 0, change the AQ value to the left and remove M from A; Otherwise, if it is 1, change the AQ value and replace both A and M and store the result in A.
Step 3: The lowest bit value of Q is set to 1 if the most important bit of 1 is 0; If it is one, the less important bit of Q is set to zero.
Step 4: Decrease the amount for counter n.
Step 5: If the value of n is 0, then we leave the loop; Otherwise, we repeat step 2 from the first.
Step 6: Rediscover the tag bit; If it is 1, add A and M; If not, the content will be in log Q and the rest in log A.

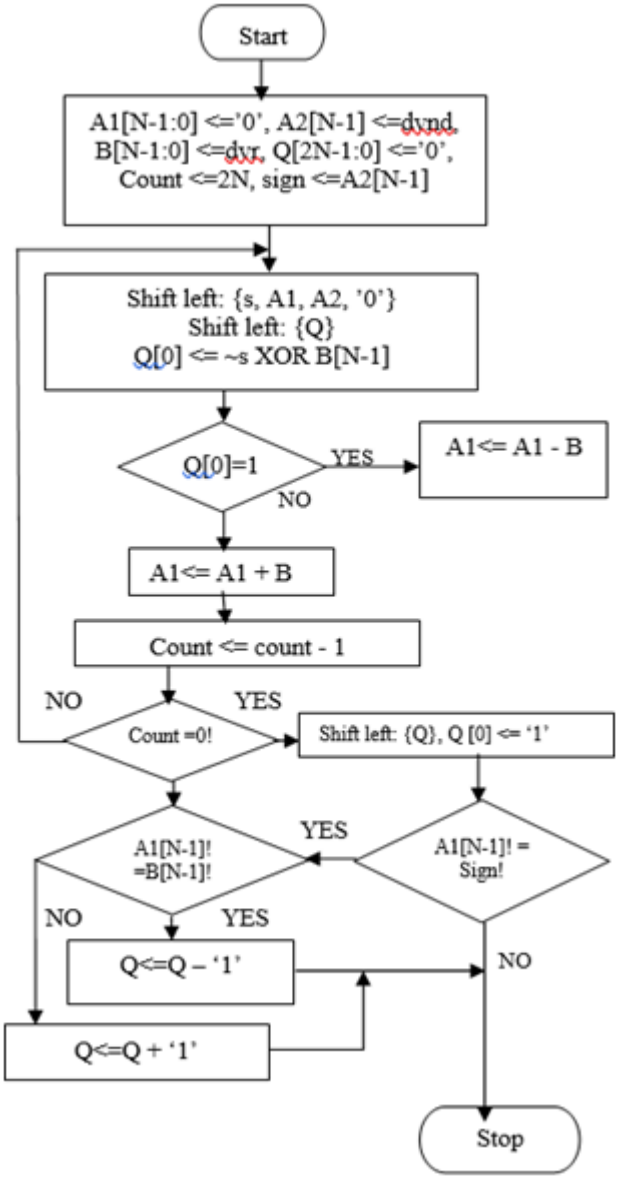

Figure 4: Flowchart for Non-restoring division algorithm for signed integer numbers

V. CADENCE TOOLOVERVIEW

Figure 5 describes the ASIC design flow in which the engineer firstly defines the features, functionalities and specifications according to the ASIC design rules, then the functionally the design has verified where they generate the RTL code using testbench. Once the RTL code and testbench are obtained then RTL code is converted into the gate-level Netlist using logical synthesis and the chip has partitioned and DFT is inserted to verify the design structure. After the DFT, in the floor planning

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The blocks are placed in the chip where it determines the size, place of the gates and connects them with the wires, next in placement standard cells are placed. In the clock tree synthesis, the timing, area, power requirements are meet with low power consumption. Finally, the global and the detailed routing is performed where in the global routing it calculates the estimated values and in the detailed routing, the actual delay is calculated and in the final verification undergoes with layout verses schematic, design rule check and logical equivalence checks are verified.

All simulated fragments have been designed to verify whether they are performing as per the requirement or not. Once done with the simulation, the next process is obtaining the power report, timing report, area report and device utilization. This segment re-produces the utilization of tools, simulations and simulated wave forms of each and every fragmentconstructed to exhibit the functionality of the different division algorithms. Simulation and the synthesis is carried out by using the Cadence RTL compiler. Cadence encounter digital execution tool is used for the ASIC implementation of algorithms.

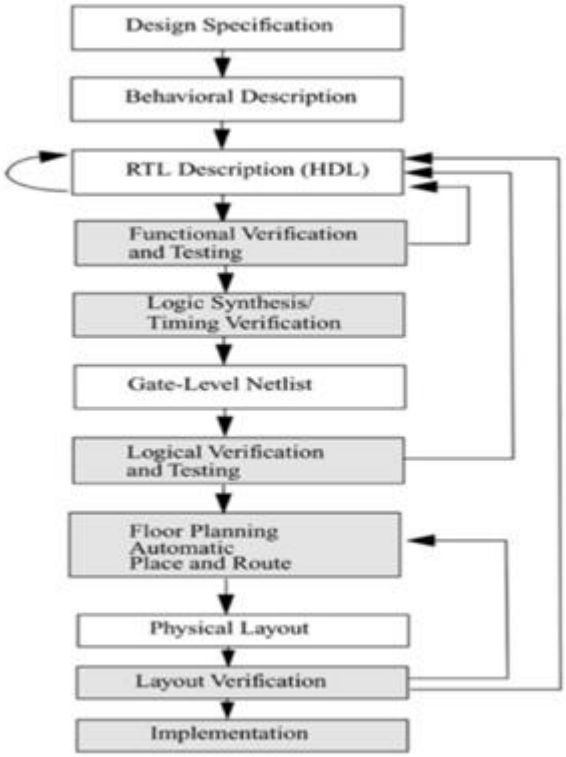

Figure 5: ASIC Design Flow

In cadence the UI (User Interface) is realistic and dependent on the structures and menus. The libraries and views contain the essential structure blocks usable in the development and plan libraries which exemplifies the plan which comprises of the cells, then the technology document which describes the semiconductor measures.

NC Launch: Graphical User Interface (GUI) is transported to design and launch the subsequent tools which has to be simulated and work the bugs out of the design. Design units are checked which executes the syntactic and static semantic using Verilog compiler. The elaborator constitutes a packing order based on information about the configuration and the instantiation in the design system, signal connectivity has been established and all objects in the design computes the initial values.

Genus: It is used for synthesis, so to use physical information to drive synthesis but are not interested in creating the physical details. It serves as an analysis tool to help you recognize the difficulties of policies, such as time and power. Design constraints are given and optimization then synthesis is made. If the constraints are not met then further modification in made. As shown below final SDC and netlist file is obtained.

Innovus: The Cadence Implementation System family of products provides an integrated solution for an

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RTL-to- GDSII design flow. Partitioning floor planning placement CTS and routing and timing closure is made in the innovus.

VI. EXPERIMENTAL RESULTS AND COMPARISION

In the Verilog hardware definition language, the above algorithms are implemented and tested for functionality (for both signed and unsigned transactions) (HDL). In contrast, all algorithms are taken from identical sources and simulated in a similar context. All prototypes were built with the cadence tool in Verilog HDL and implemented to obtain the physical layout. Figure 5 shows the simulation effects of the proposed division algorithm.Above considered algorithms are non-identical and similar type of simulation is carried out and performance parametersare compared.

A. Simulation Results

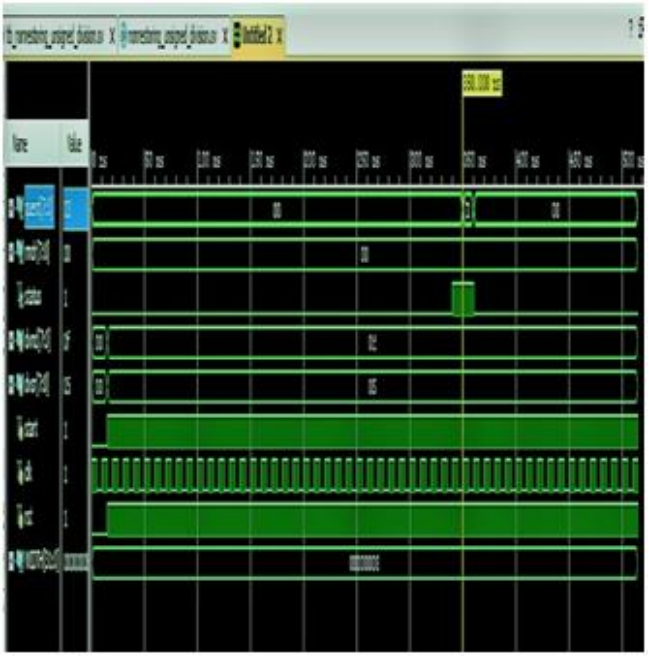

Figure 6: Simulated waveforms of the restoring division algorithms for unsigned integer numbers

All the designs that have been considered for simulation and synthetization are carried out through the cadence tool. The simulation results for the proposed division algorithm are as shown in the figure 6. There are the simulation results for different division algorithms which has designed using an FSM logic. The simulation results of restoring division for unsigned number are shown in fig 6 where the dvnd(dividend),dvsr(divisor), clk (clock),rst(reset) and start are the inputs given to the design when the clock is at the positive edge the start bit will occupy active high pin, after performing complete fsm operation the status which is output pin goes high and the outputs (quent and rmdr) is obtained. In the above example the 8-bit input for dividend is 15(0f in hexa) and divisor is 5 where the output after simulation is quent=3 and rmdr=0.Similary the same logic is applied to all the algorithms for n-bit integernumbers.

B. Overall Schematic View

The modules are practically tried after which the plan is combined. The Verilog configuration record and SDC document are given as contribution to the family instrument of rhythm. Comparing library documents are incorporated with the previously mentioned records. The reason for existing is to streamline the plan at the door level and correct the territory, timing, and force requirements.

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When the advancement is performed then the netlist record with the relating SDC document is incited for the actual format. TCL orders are applied withinside the technique to envelop the documents and improve.

Once the simulation is done the code is converted into gate level where the netlist has been generated (here the netlist generated by restoring division for unsigned is 213), using the netlist the schematic has been generated as shown in the figure 7. This Netlist contains the information of the cells used & interconnections, cell area used, and other details.

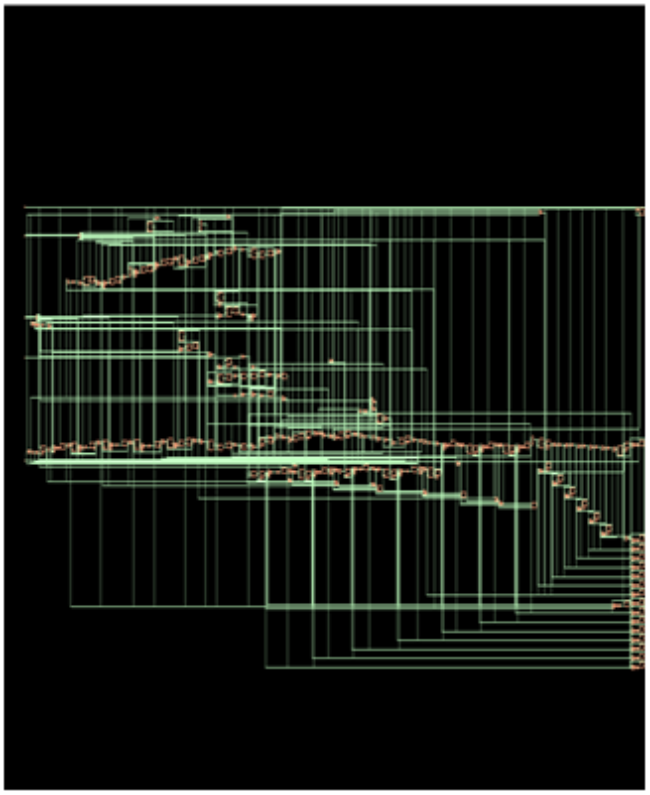

Figure 7: Schematic View of the proposed division Algorithms

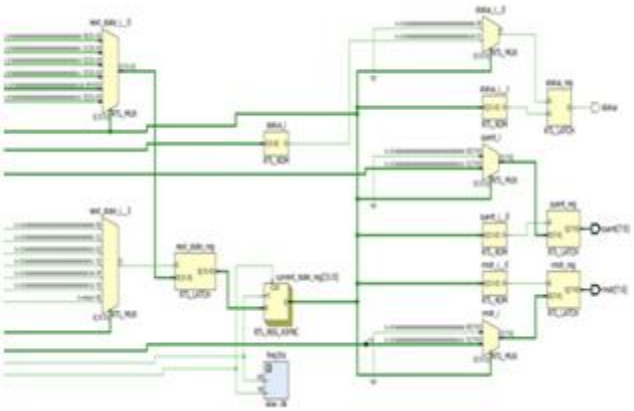

Figure 8: Detailed schematic view of the proposed division algorithm

The detailed schematic for restoring division for Signed Integer Numbers, which was checked using Verilog HDL and simulated using Cadence method, with output parameters such as power usage, latency, and area used relative to the other three algorithms. The final stage of the IC design period is tape out. If the simulation is complete, the code is translated to gate stage, where the netlist is created (in this case,

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the netlist generated by restoring division for unsigned is 213),[25][26][27] and the detailed schematic is generated using the netlist, as seen in Figure 8.

This Netlist includes information on the cells and interconnections used, as well as cell area and other data. Logic partitioning, floor plan, power plan, positioning, CTS, and routing are also exampling of physical architecture. STA is a critical phase in analyzing a design's output in terms of initialization time, hold time, retrieval time, removal time, clock delay, clock skew, and clock instability. Since all of the inspections have been completed, the specification is ready to be shipped to the foundry.

C. Layout Overview

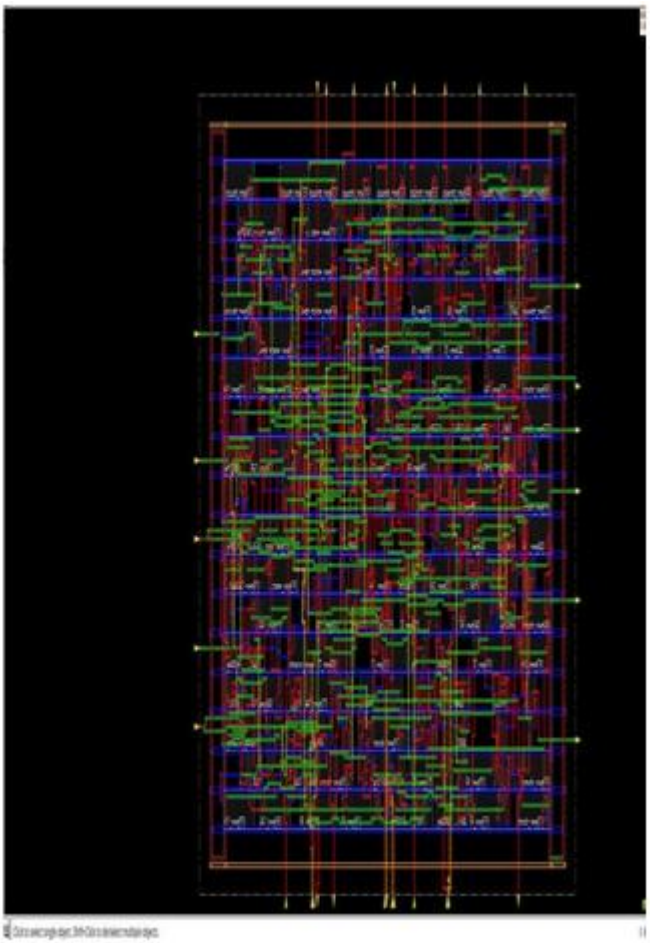

Figure 9: Layout of the proposed division Algorithms

The netlist and related documents like planning libraries, timing requirements, and LEF records are stacked into the innovus execute. At that point the floor arranging is made by giving the solid perspective proportion for the state of the cells and center usage to educate the carry out ken how thickly pressed the center should be with standard cells. The resulting step is Power arranging, it's far applied to put the force and ground ring round your circuit, and associate that ring to the columns so the phones will be associated with force and ground while they're set withinside theline.Width and separating are determined and that they should be given. Then, the standard cells are situated withinside the plan. With the clock tree union and steering, Multiple enhancements and physically moving standard cells, and incorporating supports for the circumstance, force, and zone streamlining and the great result is acquired and is appeared in the underneath picture. Then the layout has been generated has shown in the figure 9

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D.Comparison of the proposed algorithms

Table II. Comparative Results Table of the proposed algorithms

Parameter	**RUSD**	**RSD**	**NRUSD**	**NRSD**
Power(nW)	8.10x10^{+9}	11.81 x10^{+9}	9.87x10^{+9}	10.42 x10^{+9}
Delay (ps)	4296	2883	4901	3629
Area(cm)	5169226	516933.6	554510,9	654302.9
Netlist	213	320	233	285

The comparison table consists of the performance parametersi.e., power(nW), delay(ns), area(cm), and the netlist and it comprises of proposed division algorithms i.e., restoring unsigned, restoring signed, non-restoring signed and unsigned. Netlist usually consists the list of components and the nodes. The comparison of the proposed algorithms is as shown the Table II From the comparison the restoring unsigned division consumes of about 8.1nW of the power along with minimum area of about 5316922.6cm and netlist utilization is of about 213 compared to the restoring signed, non-restoring unsigned and non-restoring signed algorithms.

CONCLUSION

The design and implementation of efficient 8-bit integer division algorithms is very important and necessary. Although the division is one of the foremost difficult operation of the fundamental arithmetic operations but without division the performance of design may get degraded. In this proposed work, the different efficient 8-bit algorithms are designed and implemented on the cadence tool and it is working properly for the mentioned inputs.In the proposed work, firstly the restoring division algorithms for 8-bit unsigned and signed numbers are designed using Verilog HDL language and simulated, synthesized and implemented using the ASIC flow and the performance parameters are noted to examine the working of the algorithms. Similarly, for non-restoring division algorithms for 8-bit signed and unsigned numbers are carried used the same cadence tool to obtain the physical layout and parameters like power, delay, netlist, area is noted.

A test element has been considered which comprises of approximately 8-bit input data along with clock, reset and start.As the result of the procedures performed, it is found that when the status bit goes high after performing all states functions according to FSM logic, the output has been generated.
After synthesis of the proposed division algorithms, the comparison of performance parameters of different division algorithms has been examined and it is found that the power consumed by the restoring unsigned division is of about 0.81mW with minimum area and limited netlist of about 213 which is comparatively much lesser than restoring signed, non-restoring signed and unsigned algorithms. The gadget use synopsis showed that base assets were burned-through. At last, the ASIC execution of proposed integer division algorithms alongside different modules has been done on Cadence Encounter Digital Implementation apparatus and the GDSII record has been created.

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