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Implementation of 16-Bit Vedic Multiplier in Alu Using Verilog

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ABSTRACT:
The main focus of our proposal is to implement a Vedic multiplier in an ALU using Vedic mathematical sutras.Majority of all the DSP and Networking applications are computation intensive and energy demanding, improvements in such vital aspects could result in a marvelous upgrade to the overall performance and efficiency of existing systems. They require bothaccuracy along with high performance. Conventional multipliers were based out of direct approach designs, they provide the required functionality but are not much efficient.Vedic mathematics offers many sutras or techniques to simplify design and improve efficiency. Among many such sutras, the Urdhava Triyagbhyam sutra is employed in our design to realize a 16*16 bit Vedic multiplier to be integrated with an ALU.The key to our success is that the proposed multiplier is more power-area efficient and has reduced delay in its overall performance. The basic functionality of the project is multiplicationand the specifications are 16 bit width ALU consisting of two 16 bit inputs with a 32 bit output for multiplication, 16 bit output for other operations. The Vedic ALU is developed and analyzed in Cadence Digital systems using System verilog coding language along with ALDEC-Active HDL software for functional verifications.

1 INTRODUCTION:

Mathematics is not just a branch,it is the source and supreme of all sciences. The Applications of mathematics in the fields of DSP and networking is vital to this technological world we live in,everything depends upon the processing power and efficiency of systems.Vedic mathematics is a branch of mathematics that originated in Indian sub-continental region, it is a way of accessing the numbers and problems in a much simpler, easy way of understanding to be able to solve them rapidly. It had always been a vital integration in our lives and had been existing without even been noticed in several forms such as astrology, construction works, marine navigation and many more. The sutras in Vedic mathematics are elegant algorithms that possess the ability to solve huge mathematical computations with only human minds. They were devised in such a manner that all those huge mathematical computations could be solved easily by following a certain pattern or method by anyone having only basic mathematical knowledge.These sutras when applied to design multipliers could harness all those positives. These techniques were adapted in our project to develop an ALU unit consisting of a 16*16 bit Vedic multiplier along with other components to specifically boost up the performance of the ALU in multiplication related tasks.

2 DESIGN PRINCIPLE:

Vedic Multiplication - Urdhava Triyagbhyam Sutra:

The Urdhava Triyagbhyam sutra is one of 16 major sutras of ancient Vedic mathematics , it is a multiplication based sutras that describes the techniques for ease of multiplication.The word

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'Urdhava' translates to 'Vertical' and 'triyagbhyam' translates to 'crosswise'.It is a basic vertical and crosswise multiplication approach to solve large multiplications with ease.There are certain pattern which are illustrated below,

Consider the multiplication of two numbers a1a2a3 and b1b2b3 ,each of three digit length in Vedic mathematics approach is as follows,

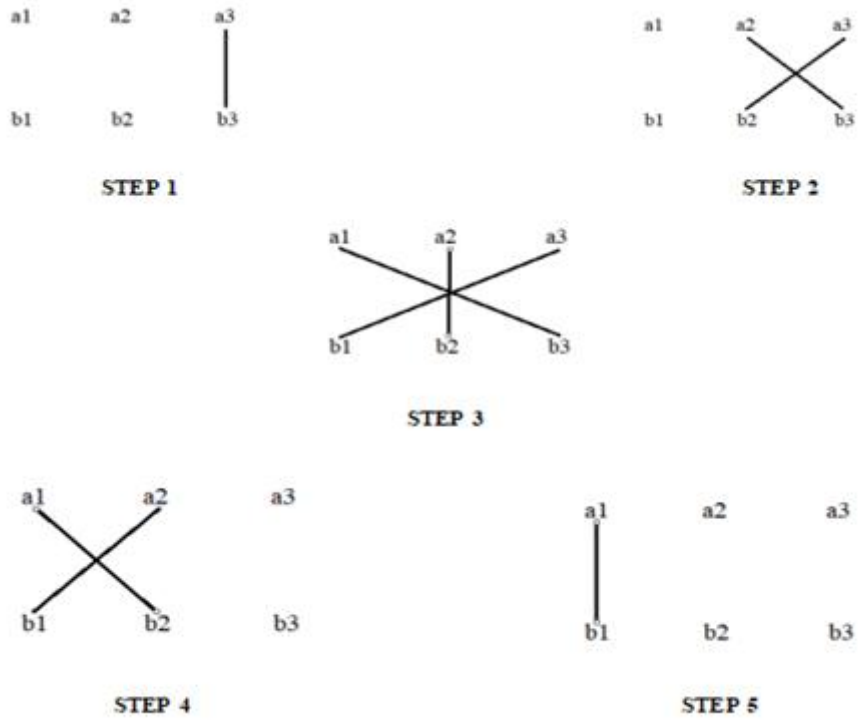

Figure:1 Urdhava Triyabhyam-Logical Steps

Steps of Explanation,

1. Vertical multiplication of last digits of two numbers.
2. Crosswise multiplication and addition of last and middle digits of two numbers.
3. Crosswise multiplication and addition of first , last and middle digits of two numbers.
4. Crosswise multiplication and addition of first and middle digits of two numbers.
5. Vertical multiplication of first digits of two numbers.

For all operations there need to be considered only last one digit of result of each step others should be carried to next step as a carry value and summed up.

3 SOFTWARE:

Cadence:

Cadence tool kit is one of the software products of Cadence Design Systems,Inc., an American multinational company headquartered in California. Cadence tool kit is a licensed software. Nowadays electronic circuits have become a integral part of many products. As the days goes on the complexity of the circuits is getting increased so its getting harder to design and verify the circuits,cadence tool kit provides a solution for this problem by helping in designing and verifying the circuits. Not only this cadence tool kit address various problems like IC packaging, PCB designing, system-level verification,custom and digital IC. It has certain tools and

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methodologies which helps us to meet certain parameters like power, time delay, area and various other constraints. It also helps achieve fast design-closure.

ALDEC:

ALDEC Active-HDL is windows based mixed language design entry and simulation software. The design entity's supports Verilog, System C, System Verilog and VHDL languages. Active-HDL is an licensed software, also provides Student Edition support. ALDEC verification suite is cost-effective and has high-performance. ALDEC-HDL verification simulator has a wide full range of applications in some industries, including communication, storage and computation. Active-HDL student edition is a'load and Go' licensed.ALDEC supports several dedicated FPGA embedded applications like Deep learning, Internet of Things, Networking and automotive ADAS. It has several pre-compiled FPGA vendor libraries for quicker access and design.It could also be interfaced with Mat lab simulation tool and Simulink tool easily.The student edition version also posses Code2Graphics and Graphics2code functionalities.It is suitable for mixed language HDL stimulation, DSP co-simulation, static design analysis and mixed signal simulations.

4 **DESIGN:**

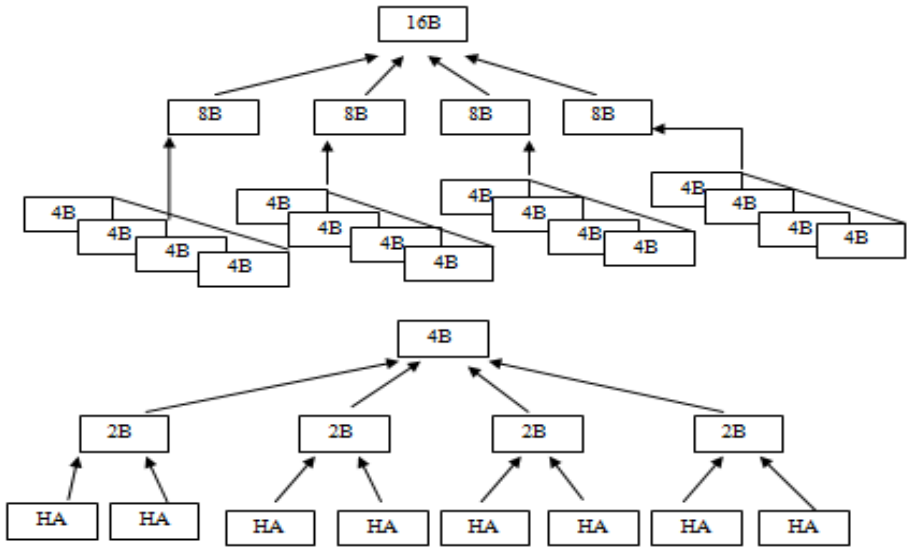

Figure:2 Design approach 16 bit vedic multiplier

The design approach of the project was bottom to top approach, so that it could be easily modulated for further usage with higher number of bits. The base operation of any multiplier design approach will be repeated addition, the project uses half adders as leaf modules to design a 2 by 2 bit Vedic multiplier module , this module in turn is used to create a 4 by 4 bit multiplier and dedicated 4 bit length, 6 bit length adders are used. This same approach is developed to realize a 16 by 16 bit vedic mathematical multiplier circuit.The architecture is highly modular for future upgrades and for debugging.This approach is more flexible to design a n by n bit vedic multiplier with the existing n/2 X n/2 lower bit width vedic multiplier.

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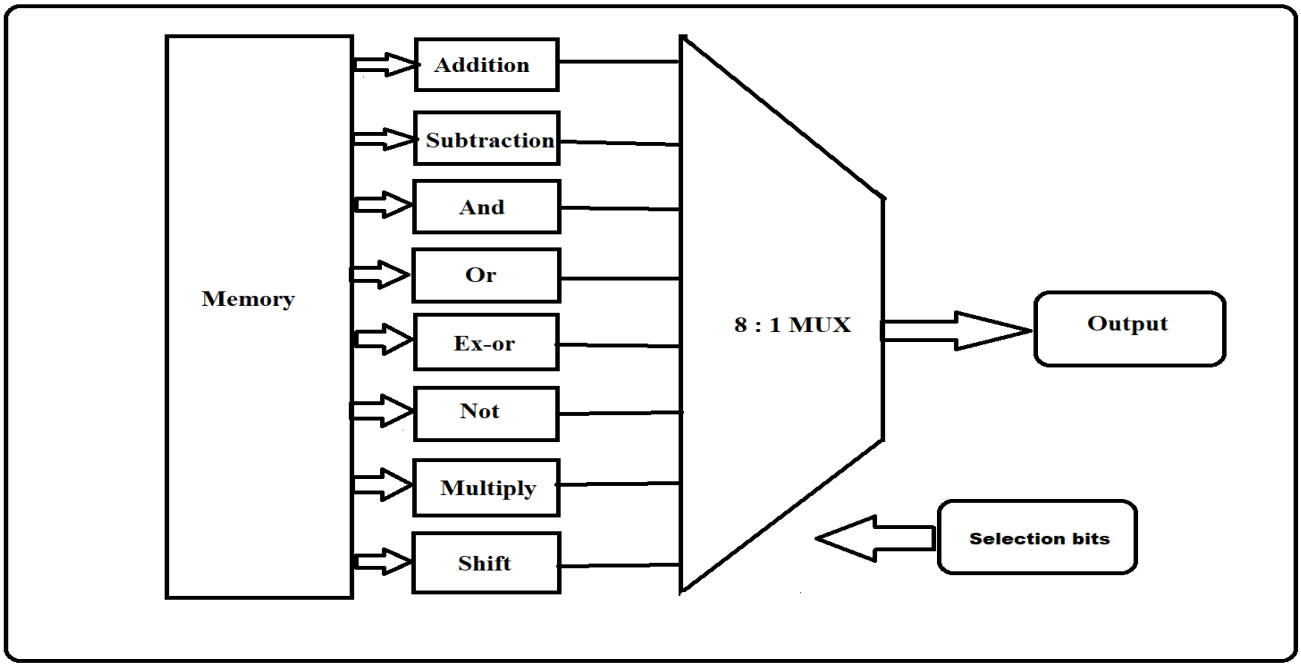

Figure:3 Overview of 16 bit ALU

A typical ALU design has been adopted and it has been integrated with a vedic multiplier. The proposed vedic multiplier design is integrated with an 16 bit wide ALU and the performance parameters of the conventional ALU built using Array multiplier is compared against the modified Vedic ALU.

Table:1 operation selection table

Selection bits N_2 N1 N_0	**Functionalities**
000	Addition operation
001	Subtraction operation
010	Bitwise and operation
011	Bitwise or operation
100	Bitwise xor operation
101	Bitwise not operation
110	Multiplication operation
111	Left shift operation

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5 RESULTSAND ANALYSIS:

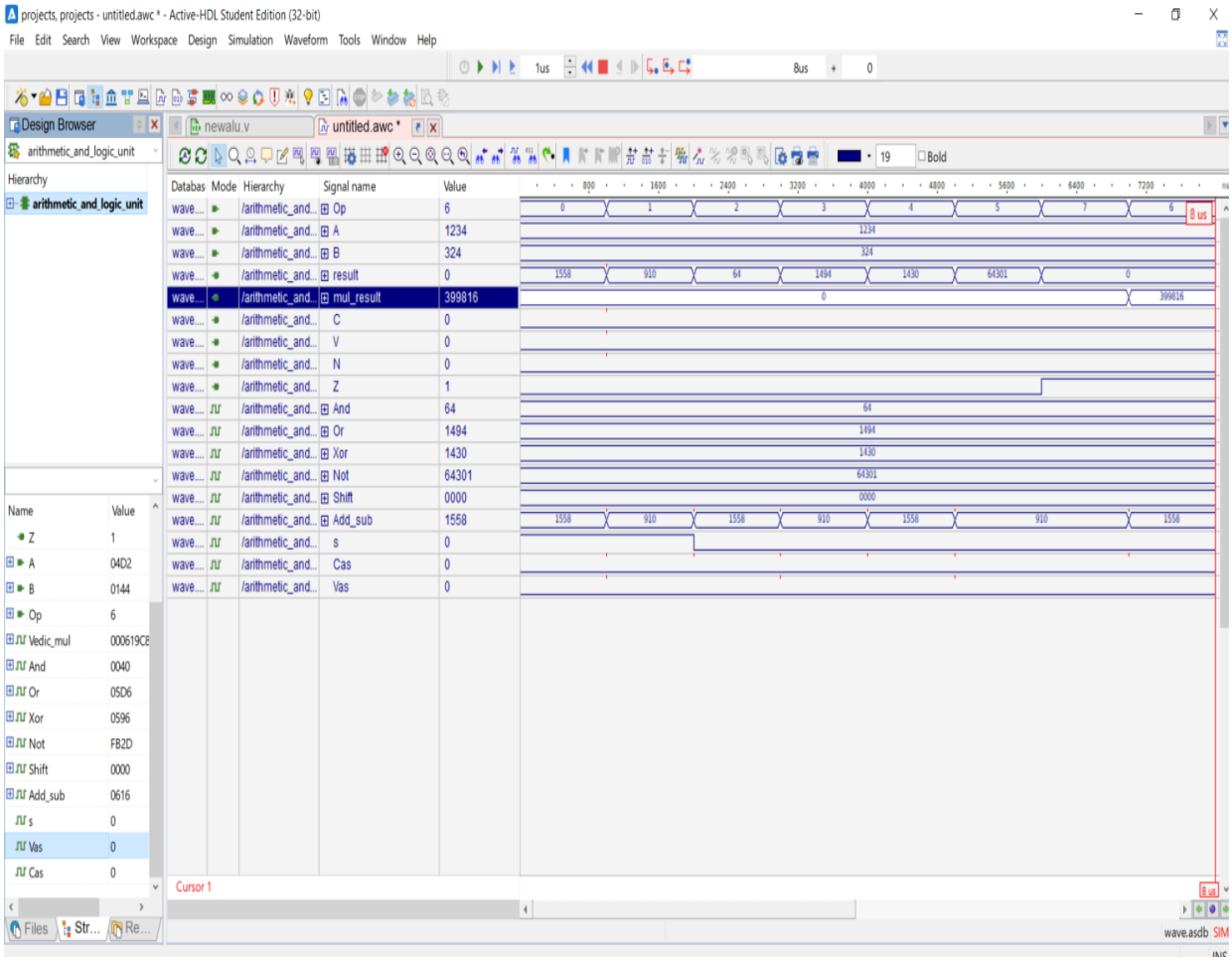

Figure 4: Simulation result for 16-bit Vedic Multiplier

when the inputs are A=1234, B=324 and selection bit is$(110)_2$, the obtained result is mul_result=399816.

6 ANALYSIS OF 8 BIT MULTIPLIERS:

The following are the parametric analysis of 8 bit multipliers.

Table:2 Parameter comparision of 8 bit multiplier

Multipliers	**Power**(nW)	**Delay**(ps)	**Area**(120nm)	**Power/Area**
Array	32,655.918	4,650	1,428	22.8683
Booth	30,125.720	4,058	1,378	21.8619
Wallace	29,008.868	3,626	1,139	25.4687
Vedic	24,480.723	3,545	1,652	14.8188

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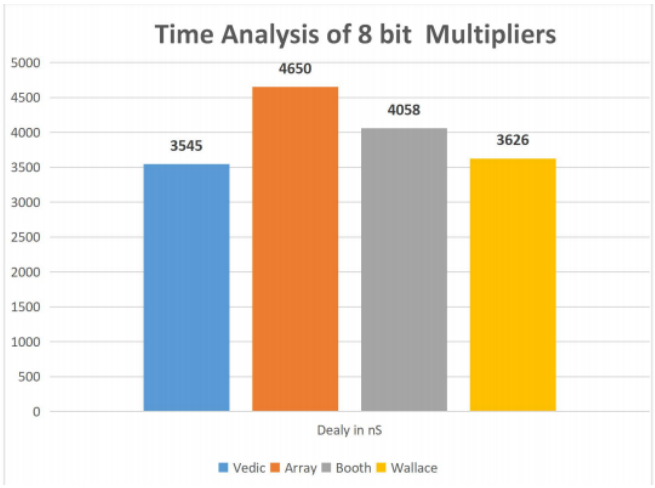

Figure:5 Time Analysis of 8 bit multipliers

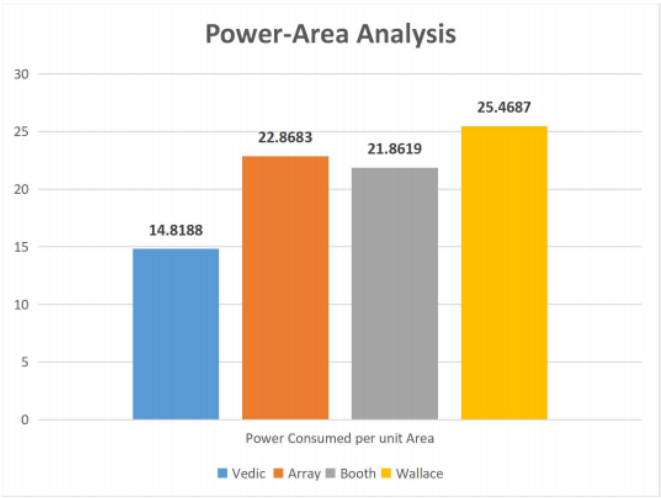

Figure:6 Power-Area analysis of 8 bit multipliers

From the above table we inferred that multiplier designed using vedic mathematics is more power-area efficient and has a reduced delay.

7 ANALYSIS OF 16 BIT ALUs:

The Vedic ALU is compared against a Conventional Array multiplier based ALU and the outcomes are described below.

Table:3 Parameter comparision of 16 bit ALUs

ALU	**Power(**nW**)**	**Delay(**ps**)**	**Area(**120nm**)**	**Power/Area**
Conventional	2,71,994.572	7465	12,488	21.7805
Vedic	2,70,149.08	6988	13,759	19.6344

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The implementation of vedic multiplier in ALU is prominent.The Vedic ALU is compared against a Conventional Array multiplier based ALU and the outcomes are described below.

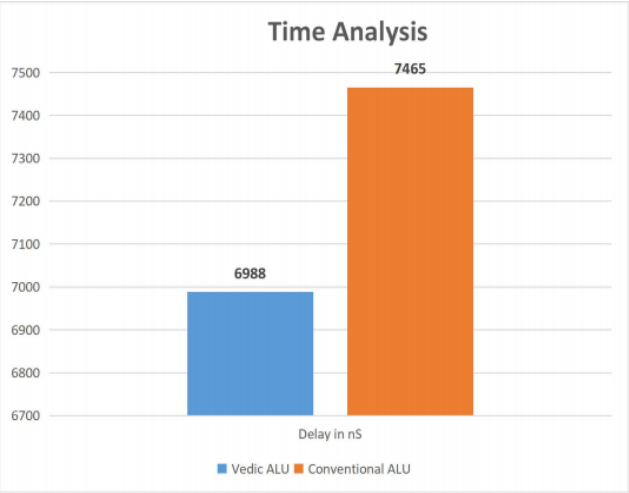

Figure:7 Time Analysis of 16 bit ALUs

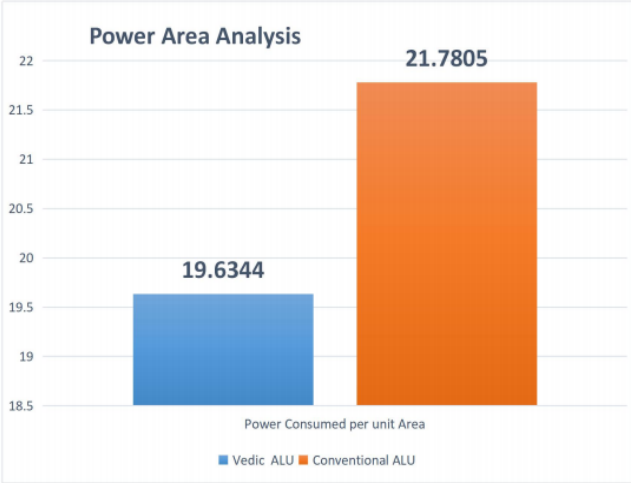

Figure:8 Power-Area analysis of 16 bit ALUs

8CONCLUSION:

Thus the proposed ALU design with Vedic mathematics approach is effective by means of Overall consumption of power,Overall delay of the system and Power consumed per unit area of the ALU.This approach can be employed as a efficient alternative to the conventional ALU designed based on array multipliers.Although the basic parameters like power,area and delay of other multiplier design methods tend to increase exponentially with the increase in the number of bits processed ,Vedic multipliers tends to moderate by showing linear graphs. The results are promising and shows a significant improvement in the performance of multiplication that is vested in an ALU with Vedic multipliers.

FUTURE SCOPE:

1.Increase the bit width and process large quantities of data.

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2.Improvement in overall power consumed and area taken by adopting latest design of 90nm,45nm and 18nm technologies.
3.Analyze the parasitic elements in our design and eliminate them to get minimize leakage power and delays.
4.Apply in real time working scenarios and prove its accuracy and precision.
5.Improve the design and promote to the fabrication of IC and PC.

REFERENCES:

[1]. "Application of Urdhava Sutra" written by A.P. Nicholas, K.R Williams, and J. Pickles, in Spiritual Study Group, Roorkee (India), 1984
[2]. "Simulation And Implementation of Vedic multiplier using VHDL code" written by S.Siva, S,Sivaramakrishnan, K.Venkatesan, Jayakumar and G.Vaithiyanathan in International Journal of Scientific &Engineering Research, Vol. 4, Issue 1, January 2013.
[3]. "Hardware Implementation of 16*16 bit Multiplier and Square using Vedic Mathematics", written by Dilip Kumar, Abhijeet Kumar and Siddhi in International Conference on Signal, Image and Video Processing (ICSIVP), 2012.
[4]. "Design and Implementation of Efficient Multiplier Using Vedic Mathematics", written by Prof J M Rudagi, Vishwanath Munavali ,RavindraPatil ,Vinaykumar Sajjan, Vishwanath Ambli IET Proc. Of Conf. on Advances in Recent Technologies in Communication and Computing, pp. 162- 166, 2011.
[5]. "Design and FPGA Implementation of Binary Squarer Using Vedic Mathematics" written by L.Sriraman, K. Saravana Kumar and T.N.Prabakar, in IEEE ICCCNT, July 4-6, 2013.