

## Multi-Level Inverter in Harmonic Mtigation using Reduced Number of Switches

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**Abstract:** This proposed paper deals with demonstrating and imitation of 13 level cascaded Multi-level Inverter (MLI) using less number of controls. The proposed system uses the topology of symmetrical multi-level inverter through separate equivalent DC sources for the control circuit. The major purpose of this proposed project is to increase the minimum number of levels of output voltage with less harmonic distortion. Optimized Harmonic Stepped Waveform technique is used to eliminate the lower order noises starting the production voltage source. Controlling angles are calculated by using Newton-Raphson method. From this obtained set of values, the firing angle which produces the least output-voltage THD will be chosen. Using these values given to MATLAB software and it's reducing the harmonics to output voltage side. After reducing the harmonics the results are taken by MATLAB software. The THD is determined by applying Fast Fourier Transformation (FFT) investigation. This reduced harmonic noises voltage is used to consumer side and produce continues voltage applications with help of reduced number of controls. This proposed multi-level inverter is used to reduce the total harmonics distortion.

**Index terms:** Cascade Inverter, Optimized Harmonic Stepped Wave form (OHSW), Fast Fourier Transform (FFT), Newton-Raphson(N-R).

### 1. INTRODUCTION:

Proposed inverter is a power electronic device that converts DC source into AC source. In recent scenario multilevel inverters plays a significant role as it has the capability of elevated power and average voltage operation [1], [4]. These inverters are considered near is the better clarification for high active performance and power value severe applications [6]. Cascade inverter production voltages create a staircase output waveform which looks like a sinusoidal waveform [3], [9]. Cascade inverters are widely used in electrical utility and for industrial drives. MLIs are of different types namely Diode clamped circuit MLI, rapid capacitor MLI, Cascaded MLI [11]. Since large number of diodes is required in diode clamped MLI and switching frequency and switching losses are high in flying capacitor MLI, cascaded MLI is preferred[2], [4].

Cascaded MLIs are used because it requires the minimum number of mechanism to attain the similar number of voltage levels; switching losses and switching stresses are less [12]. Cascaded MLIs are divided into two types namely Symmetrical and Asymmetrical structures [3]. All the DC voltage sources are equivalent the inverter is called as symmetrical MLI and the voltage sources are unequal it is called as Asymmetrical MLI [4], [7]. Harmonic reduction can be done by applying many methods like The Sinusoidal Pulse Width Modulation (SPWM) and Space Vector Pulse Width Modulation (SVPWM), Selective Harmonic Elimination Pulse Width

Modulation (SHEPWM), Optimized Harmonic Stepped Waveform technique (OHSW)[7], [10]. In this work proposed 13-level cascaded MLI is designed with reduced minimum number of IGBT or MOSFET controls and supplying it with equal DC sources in order to obtain higher level output.

This proposed project is arranged into 6 parts. Part 1 deals with introduction, gives the short history of MLI topologies. The proposed system and working of the circuit is described in part 2. Suitable harmonic reduction technique for designing MLI is mentioned in section 3. In section 4 and 5, the simulation result for 13 level inverter using the new topology is presented. Finally, the ending is presented in part 6.

## **2. CASCADED MULTI-LEVEL INVERTER:**

For the new model inverter network the necessary number of power strategy depends on the production voltage level [11], [12]. While decreasing the minimum number of power semiconductor controls the range, price, fitting area and control difficulty of the inverter circuit also decreases [6], [8]. Higher output voltage level reduces the THD without adding filters and transformers. Fig.1 said that the proposed circuit topology of cascaded multilevel inverter.

The N-R method is used for computing the desired controlling angle. This technique is one of the fastest iterative technique which is based on trial and error concept. This technique begins with an first estimate and usually converges at zero. The controlling angle which are in the choice of 0 to  $\Pi/2$  producing preferred essential voltage beside with removal order of the 5th, 7th, 11th, and 13th harmonic mechanism.

The circuit of the 13-level multilevel inverter according to this new topology consists of a single H-link which contains four controls [3] and six ladder switches connected in parallel to the H-link circuit. Each switch in the ladder circuit is provided with separate DC source [7], [3], [11]. The DC sources are symmetrical in nature [8]. The voltage level of individual DC sources is 50V which will add-up and provides a total voltage of 300V across the H-link circuit.

Every inverter topology can produce three dissimilar voltage outputs, +Vdc, 0, -Vdc by linking the DC voltage source to the AC voltage output by dissimilar combinations of the four controls S1, S2, S3 and S4. To obtain +Vdc, control S1 and S4 are twisted ON, whereas -Vdc can be obtained by spiraling ON the control S2 and S3 [3]. By turning ON S1 and S2 or S3 and S4, output source voltage is zero. The AC voltage outputs of each of the dissimilar full bridge inverter levels are connected in sequence such that the synthesized output voltage waveform is the addition of the inverter outputs. The phase voltage  $V = V1 + V2 + V3 + V4 + V5 + V6$ [5].

A diode which is connected across the switches in the H-bridge known as anti-parallel diode and it is used to prevent the switches from the ceasing of inductive current instantly, generating high voltage peaks. It acts as a free-wheeling diode and provides a path for inductive current to flow.

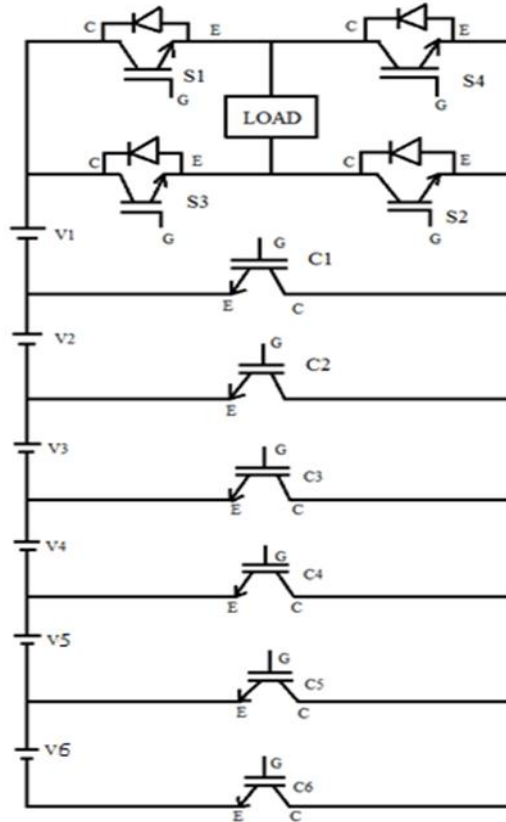


Fig.1.Cascaded multi-level inverter

The lowest number of dc sources used in the projected circuit is calculated using the formula  $S = (n-1)/2$ , where  $n$  is the number of levels in the output voltage and  $S$  is the total number of dc sources. The minimum number of power semiconductor switches required is determined with the formula  $(S+4)$ .

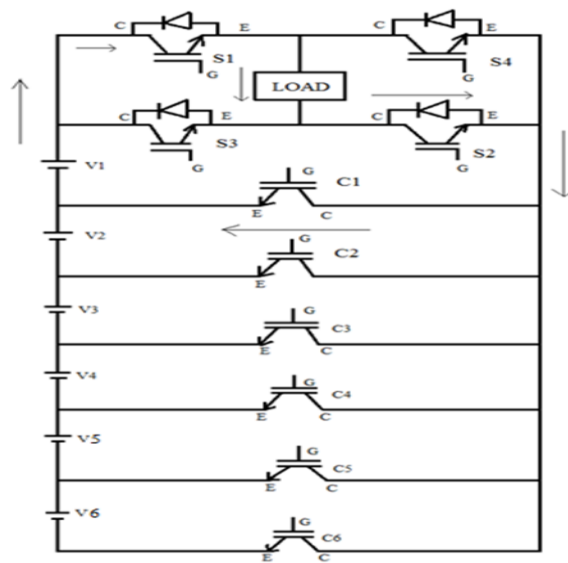


Fig.2.Positive cycle operation

Fig 2 the shows the positive cycle operation in which the load is linked across the output voltage sources after the controls S1 and S2 are twisted ON. Quantity of the voltage to be present across the load is decided by the control C1, C2..., Cn. When C1 control is turned ON the voltage E is applied across the load in positive direction. Similarly, control C2 is twisted ON to concern voltage 2E diagonally the load. That procedure is frequent awaiting peak voltage nE is obtained. Then switch Cn is turned OFF. Then the controls are turned ON in the invalidate direction from Cn to C1 to pertain a voltage of nE to E in a reduced way to form a positive sequence [13].

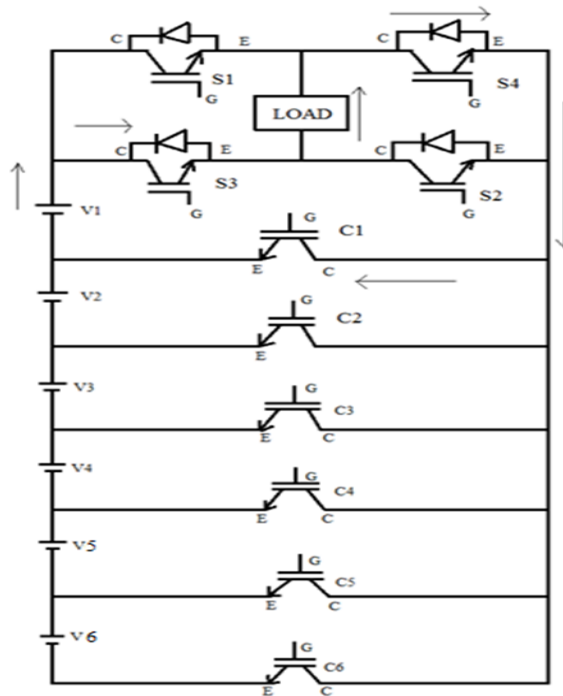


Fig.3.Negative cycle operation

Fig 3 represents the negative Cycle operation in which the load is connected across the voltage source after the switches S3 and S4 is turned ON. Quantity of the voltages to be nearby diagonally the load is determined by the controls C1, C2... Cn. When control C1 is twisted ON the voltage E is applied across the load in negative direction. This procedure is repeated until the peak voltage -nE is reached, and then the control Cn is turned OFF. Similarly, other controls are turned ON in the reverse way to decrease the voltage level from maximum voltage to minimum form a negative sequence [13].

In the table 1 the switching pattern and its corresponding voltage values are described in detail. For each level the voltage value increases and finally the desired voltage is obtained.

Table 1 represents the voltage value at different voltage point and ON state control of a 13-level multilevel inverter.

### 3. OPTIMIZED HARMONIC STEPPED WAVE FORM TECHNIQUE:

The optimized harmonic stepped wave form technique is used in this paper. Without the application of the filter circuit, THD of the output waveform is reduced by employing OHSW

technique along with the multi-level topology. For a complete cycle each switch is turned ON and OFF only once [13].

By using the optimized harmonic stepped wave form technique the switching loss and Electro-Magnetic Interference (EMI) problems can be overcome [6][15]. It is used to reduce total harmonic distortion at the production voltage from the cascaded multi-level inverter with a reduced switching frequency. The major challenge linked with OHSW method is to obtain a logical solution for the scheme of non-linear transcendental equations, which contains trigonometric term

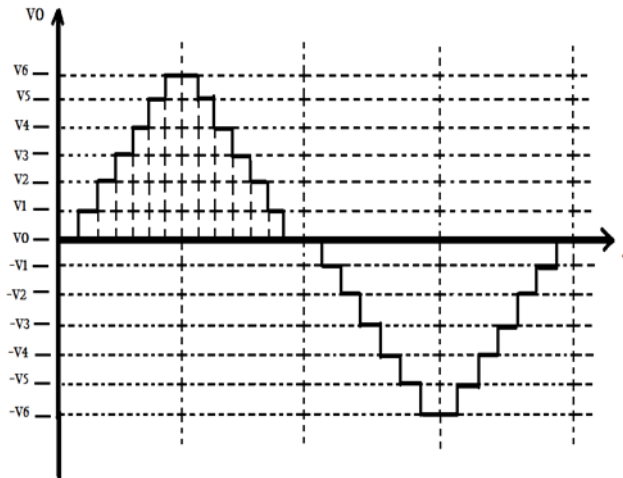


Fig.4.OHS waveform of 13 levels MLI

The fig.4 shows voltages V1 to V4 are DC voltage source, either separated DC source or regulated capacitor is used. In order to reduce harmonics in waveform three types of OHSW techniques are employed. 1) Stepped heights are changed with equal seats between steps 2) Step spaces are changed with the steps of equivalent height 3) Both step elevation and step space are changed.

The expression for the fundamental and all harmonic contents is given as,

S. NO	VOLTAGE LEVEL	H-LINK SWITCH H	LADDER SWITCH (ON)	VOLTAGE VALUE
1	6	S1 & S2	C <sub>6</sub>	$V_1+V_2+V_3+V_4+V_5+V_6$
2	5		C <sub>5</sub>	$V_1+V_2+V_3+V_4+V_5$
3	4		C <sub>4</sub>	$V_1+V_2+V_3+V_4$
4	3		C <sub>3</sub>	$V_1+V_2+V_3$
5	2		C <sub>2</sub>	$V_1+V_2$
6	1		C <sub>1</sub>	$V_1$
7	0		NIL	0
8	-1		C <sub>1</sub>	$-V_1$

9	-2	S3 & S4	C <sub>2</sub>	-(V <sub>1</sub> +V <sub>2</sub> )
10	-3		C <sub>3</sub>	-(V <sub>1</sub> +V <sub>2</sub> +V <sub>3</sub> )
11	-4		C <sub>4</sub>	-(V <sub>1</sub> +V <sub>2</sub> +V <sub>3</sub> +V <sub>4</sub> )
12	-5		C <sub>5</sub>	(V <sub>1</sub> +V <sub>2</sub> +V <sub>3</sub> +V <sub>4</sub> +V <sub>5</sub> )
13	-6		C <sub>6</sub>	(V <sub>1</sub> +V <sub>2</sub> +V <sub>3</sub> +V <sub>4</sub> +V <sub>5</sub> +V <sub>6</sub> )

$$V(\omega t) = \sum H_n(\alpha) \sin(n\omega t) \quad (1)$$

Where,

$$H_n(\alpha) = \begin{cases} \frac{4E}{n\pi} \sum_{k=1}^m \cos(n\alpha_k) & \text{for odd } n \\ 0 & \text{for even } n \end{cases}$$

E– DC voltage source,

m– number of DC sources, α<sub>k</sub> – switching angle of level k

From Equation (1) shows that odd number of harmonics (3rd, 5th...) and non-triplen odd harmonics (5th, 7th...) can be eliminated by solving it for required no. of harmonic order.

The equation 2 solution above up to nth harmonic order we get following equations

$$\cos\alpha_1 + \cos\alpha_2 + \dots + \cos\alpha_k = mM/4$$

$$\cos 3\alpha_1 + \cos 3\alpha_2 + \dots + \cos 3\alpha_k = 0$$

$$\cos 5\alpha_1 + \cos 5\alpha_2 + \dots + \cos 5\alpha_k = 0$$

....

....

$$\cos n\alpha_1 + \cos n\alpha_2 + \dots + \cos n\alpha_k = 0$$

Newton Raphson technique is used to resolve the mathematical equations to find the controlling angle.

#### 4. SIMULATION CIRCUIT:

For simulation process and programming MATLAB software is used. The firing angles for the IGBTs are calculated by executing the MATLAB program. Fig 5 consists of consists of one H-bridge and six ladder switches. To acquire the desired voltage, symmetric DC sources are connected in series.

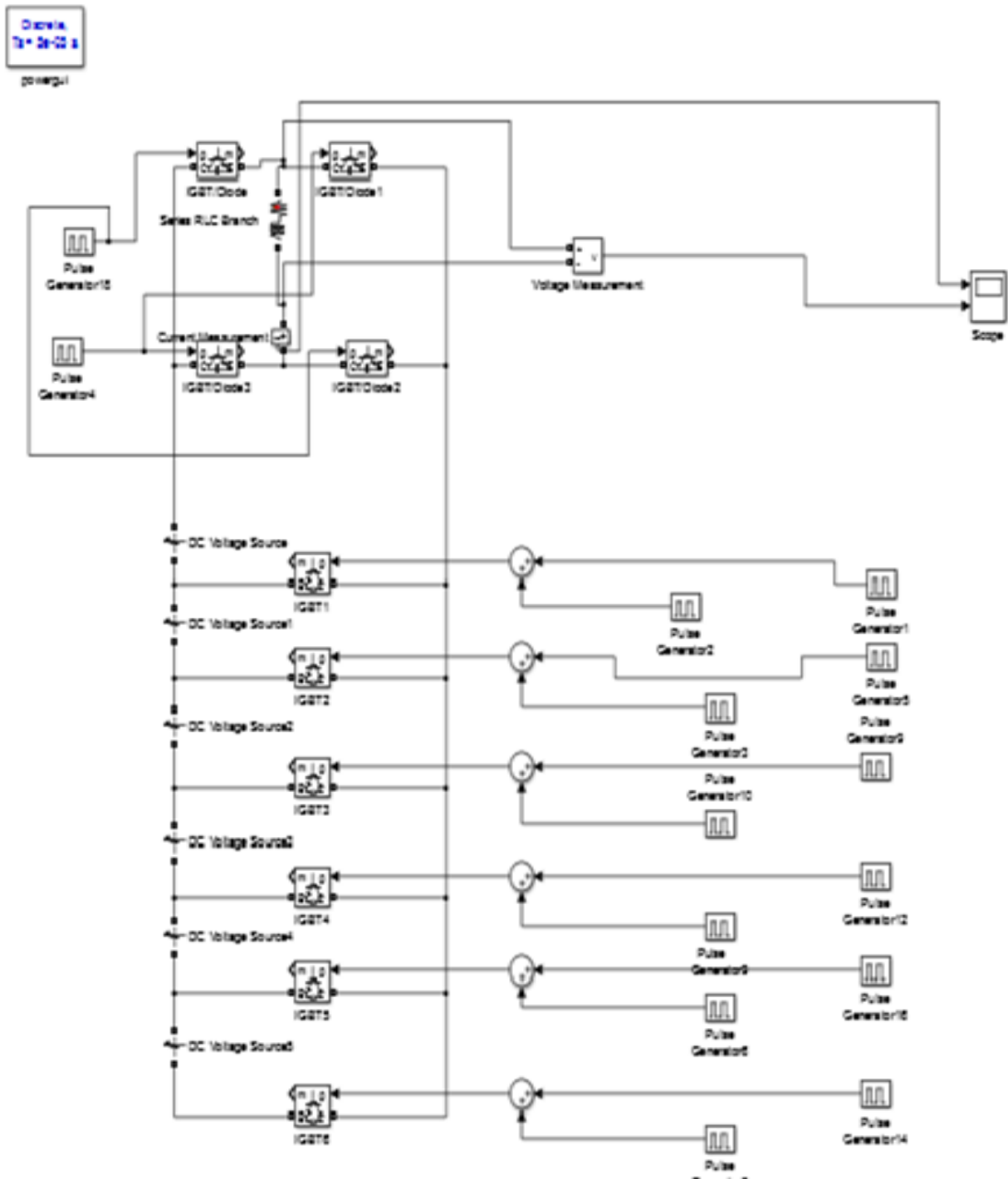


Fig.5. Simulation diagram of 13 level multi-level inverter.

The required voltage is determined by controlling the ladder switches and H-link switches.

The switches in the H-bridge are triggered using pulse generator. The firing angles for the ladder switches obtained from the MATLAB program is shown in Table 2.

Table

2. Firing angle values for the ladder switches

Firing angle	Value	Firing angle	Value
$\alpha_1$	5.9940	$\alpha_7$	113.0040
$\alpha_2$	18.7488	$\alpha_8$	133.0002
$\alpha_3$	24.9984	$\alpha_9$	139.7502
$\alpha_4$	40.2498	$\alpha_{10}$	155.0016
$\alpha_5$	46.9998	$\alpha_{11}$	161.2512
$\alpha_6$	66.9960	$\alpha_{12}$	174.0006

5. SIMULATION OUTPUT:

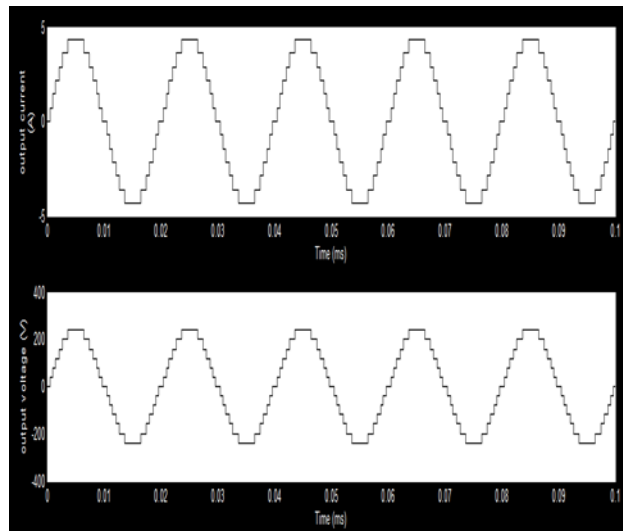


Fig.6. Output current and voltage waveform for 13 level multi-level inverter.

The output voltage and output current waveform has 13 levels.

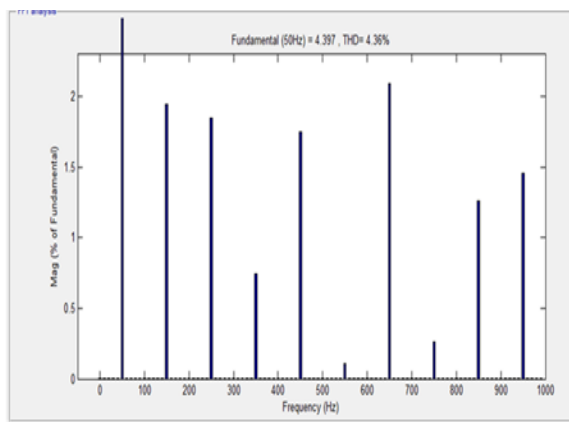


Fig.7. FFT Analysis of output current



The obtained solution sets for firing angles are limited based on the level and series of modulation level index which gives the appropriate solutions for controlling angles. The FFT is used to obtain the harmonics level of spectrum the production voltage source and output current waveform. From the obtained result it is obvious that total harmonic distortions are radically reduced when compare the MLI level is increased.

The THD value obtained using MATLAB R2013a software simulation process is 4.36%.

## 6. CONCLUSION:

Thus the cascaded MLI of 13 levels with minimum number of control is proposed, simulated and analyzed. The simulation results show that sinusoidal voltage is obtained with less distortion. After applying OHSW method harmonic content is 4.36%.

## 7. REFERENCE:

- 1) Zhong Du, Leon M. Tolbert, BurakOzpineci and John N. Chiasson,” Fundamental Frequency Switching Strategies of a Seven-level Hybrid Cascaded H-Bridge Multi-level Inverter”, IEEE Transactions on Power Electronics, Vol-24.No.1, pp.24-33 , Jan 2009
- 2) RasoulShalchiAlishah, Seyed Hosseini, EbrahimBabaei, Mehran Sabahi, “Optimum design of new cascaded switch ladder multilevel inverter structure”, IEEE Transactions on Industrial Electronics, DOI: 10.1109/TIE.2016.2627019
- 3) ShaliniTahunguriya, A. Rakesh Kumar, T. Deepa, “Multilevel Inverter with Reduced Number of Switches and Reduction of Harmonics”, Middle-East Journal of Scientific Research 24, pp. 184-191, 2016.
- 4)AtaollahMokhberdorani, Ali Ajami, “Symmetric and Asymmetric Design and Implementation of New Cascaded Multilevel Inverter Topology”, IEEE Transactions on Power Electronics, DOI: 10.1109/TPEL.2014.2302873, 2014.
- 5) Krishna Kumar Gupta, AlekhRanjan, PallaveeBhatnagar, Lalit Kumar Sahu, Shailendra Jain, “Multilevel Inverter Topologies with Reduced device Count”, IEEE Transactions on Power Electronics, Vol.31, Issue.1, DOI: 10.1109/TPEL.2015.2405012, pp.1-17, Jan 2016.
- 6) Venkatesh, Sri V.V.N.Murthy, “Modelling and Simulation of Multilevel Inverter Using Switched Series and Parallel DC Voltage Sources”, International Journal of Advanced and Innovative Research”, ISSN: 2278-7844, pp. 275-279, 2012.
- 7) Mariusz Malinowski, K. Gopakumar, Jose Rodriguez, Marcelo A. Perez, “A Survey on Cascaded Multilevel Inverters”, IEEE Transactions on Industrial Electronics, Vol.57, no.7, pp.2197-2205, July 2010.
- 8) AlirezaNami, FiruzZare, Arindam Ghosh, FredeBlaabjerg, “A Hybrid Cascaded Converter Topology with Series-Connected Symmetrical and Asymmetrical Diode –Clamped H-Bridge cells”, IEEE Trans Power Electronics, Vol.26, no.1, pp.51-65, Jan 2011.

- 9) G. S. Konstantinou, M. S. A. Dahidah, V. G. Agelidis, “Solution Trajectories for Selective Harmonic Elimination Pulse-Width Modulation for Seven-level wave forms: analysis and implementation”, IET Power Electron, Vol.5, Issue.1, pp.22-30, 2011.
- 10) Amirhossein Moeini, Hui Zhao, Shuo Wang, “ A Current Reference Based Selective Harmonic Current Mitigation PWM Technique to Improve the Performance of Cascaded H-bridge Multilevel Active Rectifiers”, IEEE Transactions on Industrial Electronics, Vol 65, issue 1, Jan 2018
- 11) Jih-Sheng Lai, Fang Zheng Peng, “ Multilevel Converters – A New Breed Of Power Converters”, IEEE Transactions On Industrial Applications, Vol.32, No.3, pp.509-517, May/June 1996.
- 12) Jose Rodriguez, Jih-Sheng Lai, Fang Zheng Peng, “Multilevel Inverters: A Survey Of Topologies, Controls and Applications”, IEEE Transactions on Industrial Electronics, Vol.49, no.4, pp.724-738, Aug 2002.
- 13) Sivakumar. N, Sumathi. A, Revathi. R, “THD Analysis of a Thirteen Level Asymmetric Hybrid Cascaded Multilevel Inverter for Industrial Application”, World Eng. & Appl. Sci. J., ISSN: 2079-2204, DOI: 10.5829/IDOSIWEASJ.2015.6.2.22150, 2015..
- 14) Rokan Ali Ahmed, S.Mekhilef, Hew Wooi Ping,  
“New Multilevel Inverter Topology With Reduced Number Of Switches”, International Middle East Power system Conference, Vol 25, pp.565-569, 2010.
- 15) Somayeh Alilu, Ebrahim Babaei, Sara Laali, “ A New General Topology for Cascaded Multilevel Inverters With Reduced Number of Components Based on Developed H-bridge”, IEEE Transactions on Industrial Electronics, Vol.61, no.8, pp.3932-3939, Aug 2014.