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Design Optimization of Low power VLSI Circuits in Deep Submicron Technology

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Abstract: This paper explores the effect of scaling for low energy and high efficiency of demand and as difficulties of SOI circuits designing. This paper presents the design of a 45 nm SOI MOSFET and surveys the effect on various instrument parameters of the variant of channel doping and gate oxide thickness. Characteristics have been acquired for the suggested MOSFET by considering the most helpful channel doping and TOX values. The Visual TCAD system of used to simulate devices and extract parameters.

Index Terms: *CMOS, SOI, low-power, High performance, Circuit design.*

I. INTRODUCTION

In telecommunications, audio, video, avionics and a range of mobile electronic consumer products, real-time digital signal processing (DSP) has become increasingly common. With DSP becoming increasingly common[1], there have been growing requirements for multipliers and dividers implementing VLSI hardware that are quicker and more effective in the region. The logarithm emerged from a desire to make arithmetic computations simpler. Multiplication and division[7] can be simplified to the point of addition and subtraction by using logarithms; in addition, energy and root issues are decreased respectively to multiplication and division

|Requirements of performance and power consumption in VLSI circuits over the past few decades, the notion of device scaling has been continuously end [1]. However, conventional device structures are nearer basic physical boundaries, such as bulk MOS transistors [2]. As the size of the device shrink to below the submicron, the boundaries at standard MOS[12] constructions because of the strong at short channel effect and the quantum theorem effect, they become more pronounced, restricting the increase in effectiveness[11]. Therefore, it is vital to look at new device structural model to promote the growth of the VLSI design industry in nano-scale production.. The silicon-on-insulator (SOI) transistors may an outstanding modelling technology to choice for nano-scale circuit design. [1].

SOItechnologies to shown mote advantages over bulk silicon technology, such as low parasite junction ability, ele vated soft error immunity, removal of CMOS latch-up, no threshold voltage degradation with body effect, and simply device insulation process [3].

Because of its intrinsic structure, SOI has recently drawn specific attention of the short channel impact and improved current drive capacity [4]. at the focus, though, is on the device level. The advantages of SOI transistors

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come at an additional door (back-gate) cost, leading in elevated gate capability, dual leakage channels, and hard at front and back gate coupling, complicating the circuits' layout[5].

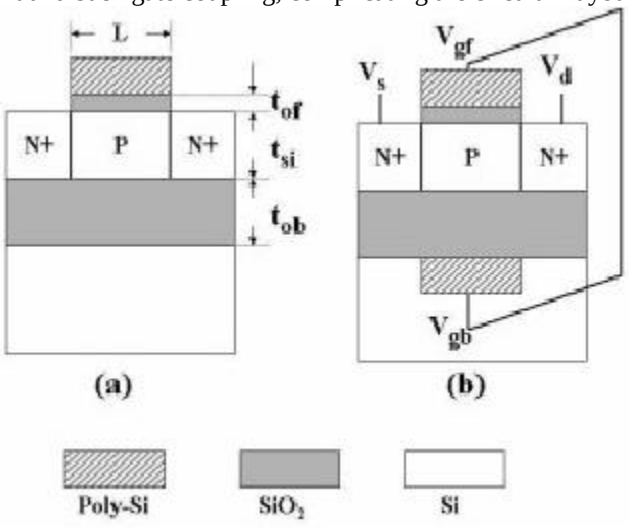

Fig 1: SOI MOSFET

trying to address SOI's design issues in this document. The demand and challenges of SOI circuits in the nano-scale region for low-power high-performance.

II.LITERATURE REVIEW

Fig.1 indicates the cross-section view of a fully depleted SOI transistor in which tof, tsi, and tob represent Oxide at the front gate, film of silicone and oxide density at the back gate[6]. Tof is usually considered as the minim um oxide of high performance density. Usually the tob is bigger than the tof. SOI displays a floating body effect. If the silicon film is thicker than maximum depletion width is considered to be a partially depleted SOI at MOSFET[8-10].

The silicon substratum produces Silicium island with silicon dioxide sandwiched [16]Fig. 2(a). To define the source at drain cavities a reactive ion is used at another low-temperature ELO the remaining islands of silicon as a plant for the development of S / D contact . In the S / D cavities Fig, polysilicon which filled . Wet etching for the removal of dummy doors Fig. 2(e) from above is considered

III .LOW POWER ANALYSIS

3.1: DYNAMIC POWER

The power consumed by a System on Chip is sum dynamic power and as well as static power[18].

Dynamic powers at the power to be dissipated/consumes once the fabrication at active mode[13]. Whenever a device is in active mode the ability dissipated within the device is termed as Static power, however the signal values are unchanged[14]

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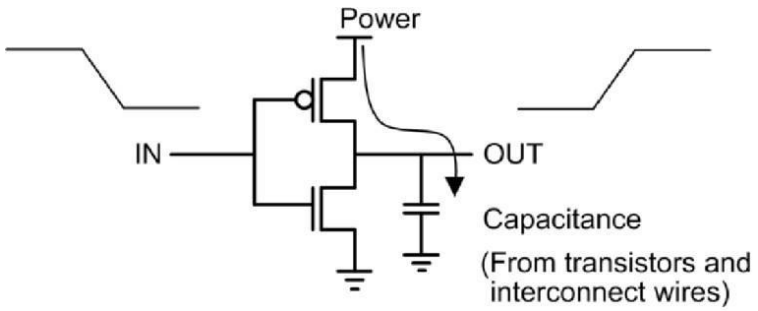

Fig.2: DYNAMIC POWER

$$P_{Short-circuit} = I_{SC}\, V \quad \text{..... (2)}$$

$$P_{Leakage} = V_{dd}\,(I_S I_G I_D) \quad \text{..... (3)}$$

$$P_{Total} = P_{Dynamic} + p_{Leakage} \quad \text{..... (4)}$$

$$P_{Total} = (\alpha C_L V^2{}_{dd}\, f_{CLK}) V_{dd}\,(I_S I_G I_D) \quad \text{..... (5)}$$

The voltage applied to the door terminals regulates the electrical field, which determines the quantity of present flow through the channel. MOSFET[15] Double Gate has two operating modes as shown in Fig.2

IV.RESULATS

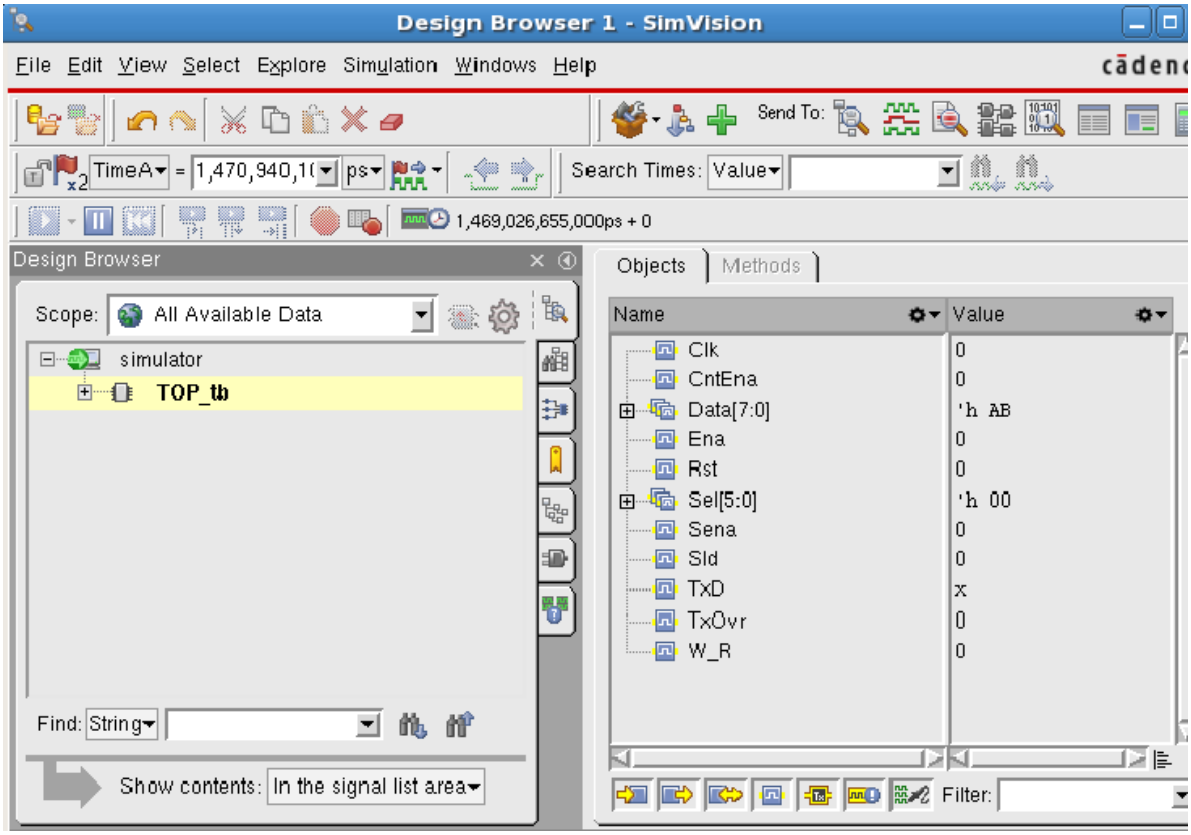

Fig 3: Impact on Channel Doping IOFF

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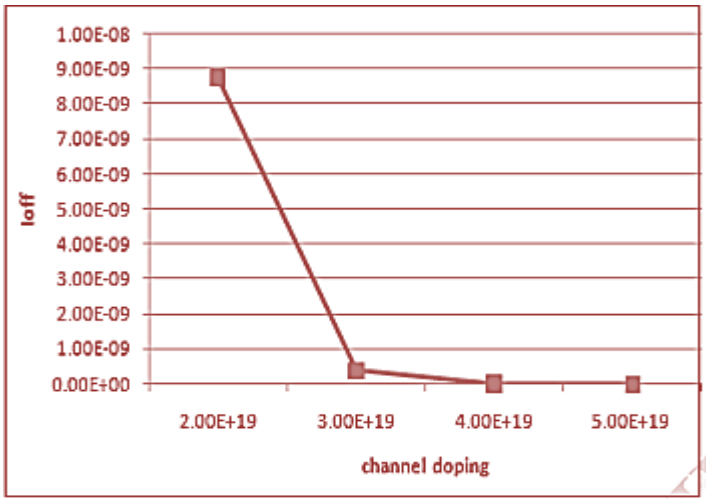

Fig4: Impact on Channel Doping on VTH

V.CONCLUSION

From the above assessment, we can conclude that owing to the brief channel impacts that slink in at smaller door lengths as the systems are scaled down, the off-current develops a significant problem. Channel engineering can be used to control the leakage within permissible limits, but channel doping cannot be enhanced beyond a certain stage as a trade-off between ION and IOFF is essential. High concentrations of doping can lead to degradation of carriers ' mobility in the channel.

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