Annals of R.S.C.B., ISSN:1583-6258, Vol. 25, Issue 4, 2021, Pages. 3396 - 3403
Received 05 March 2021; Accepted 01 April 2021.

Design Low Power of 8-Bit Alu in 45nm Using Gdi Technology

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ABSTRACT
Arithmetic and logic unit is commonly known as ALU, is an important device in all the digital devices, it is the heart, which performs all the computations that user needs from the device. By expanding the interest for upgrading the capacity of processors to deal with the more troublesome and testing undertakings has brought about the combination of a few processor cores into one chip. All things considered, the load on the processor is more in the conventional framework. An ALU actualized a central building block of the CPUof a computer. It is a combinational rationale unit that plays out its intelligent or math tasks. ALU is getting more modest and more troublesome these days to empower the advancement of all the more powerful yet more modest computers. In, this task, an exertion is made to plan a 8-digit ALU in GDI the rationale that can perform 16 alternatives in both 90nm and 45nm[1][2], the other output of these activities are given to a MUX where just the ideal output is chosen and shown. Speed, power utilization, accuracy are the vital components to be taken while during the plan of the ALU. The 8-cycle ALU has been planned, actualized and analyzed in standard gpdk45nm and 90nm utilizing the CADENCE tool. The boundaries like force, delay have been calculated in both 45the nm and 90nm and have been thought about.

I.INTRODUCTION

The performance of an advanced circuit is determined by its speed in generating output when giving information. The best-known innovation for computer-aided circuit planning is the CMOS innovation. With the improvement of CMOS logic, there has been a growing need to advance the circuit in terms of speed. One strategy considered has been to use PTL, which uses fewer gates to understand an activity. The transmission gate is one of them, which is usually a mixture of PMOS and NMOS transistors that are also assigned. The GDI cell addresses a different type of inter-communication technology, which appears to be of the CMOS type, but which stands out in reserve compared to the information terminals. The fundamental focal points of PTL over traditional CMOS configuration are as per the following

1) Lesser number of transistors brings about low force dissemination and lesser delay.
2) Minimum number of transistors, so the area is smaller and the connection effects are less.

However, PTL technologies also suffer from two major problems, such as: increased static dissipation and reduce circuit speed when operating at low power.

BASIC GDI CELL

From the start, the essential cell helps one to remember the standard CMOS inverters, yet there are some significant differences. 1) Bulks of both Negative Metal Oxide Semiconductor and Positive channel Metal-Oxide Semiconductorare associated with N or P (individually), so it very well may be discretionarily one-sided interestingly with a Complementary Metal-Oxide Semiconductor inverter. The GDI cell structure is not the same as the current PTL procedures. It should be commented that not the entirety of the capacities are conceivable in the standard p-well CMOS measure however can be effectively executed in twin-well SOI or CMOS advances. 2) The GDI cell contains three sources of info: G (normal entryway contribution of PMOS and NMOS)The GDI method is based on the use of a simple cell as shown in fig 1

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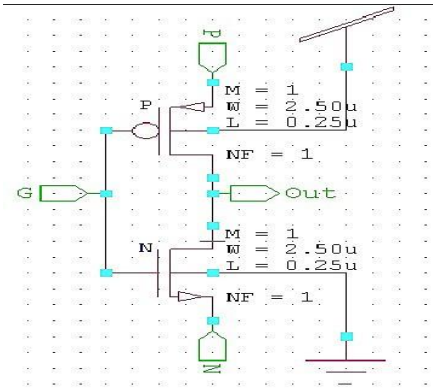

Fig 1 Basic GDI cell

II. POWER DISSIPATION IN CMOS DIGITAL CIRCUITS

The NMOS logic consumes power while the transistor is off, since the load resistor and n type network have a current path from Vdd to Vss.

Complementary Metal-Oxide Semiconductor logic uses less energy than Negative Metal Oxide Semiconductor logic circuits because Complementary Metal-Oxide Semiconductor only uses energy when it changes ("dynamic energy"). In a typical ASIC in a modern 90 nm process, the change in power can take 120 seconds and occur every ten nanoseconds.

Static Complementary Metal-Oxide Semiconductor gates are very energy efficient because they emit practically no current when inactive. As CMOS technology has fallen below the submicron level, power consumption per unit area of the chip has increased dramatically.

There are two types of power dissipation in CMOS digital circuits: maximum power and average power

The peak performance affects both the life and the performance of the circuit. Excessive spontaneous instantaneous current from the power supply leads to a voltage drop on the power rails (GND and Vdd). Because of its impedance, this large current leads to increased power loss in the power cables. Therefore, this power consumption leads to overheating of the circuit, which reduces the reliability and life of the circuit. In addition, a voltage drop in the power lines will affect the performance of the circuit and lead to errors and faulty digital outputs. Average power is important in calculating battery life and weight. It is categorized intotwo types:

Dynamic Dissipation

Any time they are replaced, CMOS circuits consume energy by charging different load limits. The current flows from the VDD to the loading capacitance in a complete CMOS logic model, which then passes from the loading capability (CL) to the ground during release. Consequently, Q = CLVDD communicates typically from VDD to field. Double this by exchanging repeated charging capacitors, so as to obtain the power of the client, and then re-enhance the standard voltage to enable the swap power to be engulfed by a CMOS – stage three and transistor failure.

Static Dissipation

Because of the direction of the reverse slope between the propagation areas and pits (e.g., p-type dispersion versus n-wells), pits and substrate, small reverse leakage currents are encapsulated (e.g., pits versus substrate). In the cutting edge technique, the diode leakage is minuscule contrasted with the passage and sub-limit currents, so it tends to be ignored in force computations.Pstat=$V_{DD} \times I_{DD}$

Another type of power consumption has become an important subsystem related to the digital framework. An ALUis a necessary part of a computer processor. It is a rational combinatorial unit that develops its methodological and coherent activities. ALUs with different bit widths are most often required in VLSIs from ASICs`. Arithmetic logic unit is getting more and more humble and mind-boggling these days to further the advancement. Figure 1. Shows the Block graph of arithmetic logic unit

Short-Circuit Power Dissipation

Since PMOS and NMOS have a small increase/ dropping time, the two halves are switched on during the progress for a short time, e.g. from start to finish, where the current finds a way from VDD to Earth. The short power spread increases with the semiconductors' rising and dropping seasons.

In the 1990s, another form of electricity consumption was huge as the on-chip cables leaked and long cables became robust. CMOS gates close to the end of these cables display mild data bursts. NMOS and PMOS logic

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networks are not completely conductive and existing streams directly from VDD to VSS are at the core of these innovations. This is called leverage the power used in this way. This effect is amplified by a neat layout that prevents the sadly decided thin cables, but leverage may be the cornerstone of dynamic CMOS efficiency.
$P_{s.c.} = \alpha V_{dd} F$ (input-transition, output-transition)

4. LOW POWER VLSI TECHNOLOGIES

Numerous alterations might be applied to the cycle innovation to diminish power dissemination. These adjustments incorporate lessening the edge voltage, decreasing the base door length, and expanding the number of metal layers.

5. BLOCK DIAGRAM OF ALU

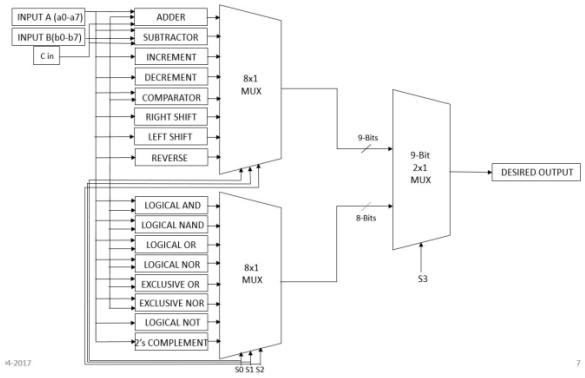

Fig 2 Block diagram of ALU

Arithmetic block: This block is utilized to perform math tasks, for example, expansion, deduction and correlation. The center of the number-crunching block is adder. In the engineering introduced, the snake utilized is adjusted convey select viper.

Logic block: This block is used to perform simple bitwise logic operations such as NOT, XNOR, XOR, NAND, AND, OR and etc.

6. DESCRIPTION OF ALU

In this sub topic we will discuss about each block used in ALU in detail.

TRUTH TABLE FOR ALU:

Table1: Truth table of ALU

S0	S1	S2	S3	OPERATION
0	0	0	0	ADDITION
0	0	0	1	LOGICAL AND
0	0	1	0	SUBTRACTION
0	0	1	1	LOGICAL NAND
0	1	0	0	INCREMENT
0	1	0	1	LOGICAL OR
0	1	1	0	DECREMENT
0	1	1	1	LOGICAL NOR
1	0	0	0	COMPARATOR
1	0	0	1	EXCLUSIVE OR
1	0	1	0	ARITHMETIC RIGHT SHIFT
1	0	1	1	EXCLUSIVE NOR
1	1	0	0	ARITHMETIC LEFT SHIFT
1	1	0	1	LOGICAL NOT
1	1	1	0	REVERSE
1	1	1	1	2's COMPLEMENT

The above table .1 shows the truth table of the ALU, based on the select lines any one particular operation is selected and is displayed as the output.

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III.WORKING OF THE ALU:

Here in this work, we have implemented the above block diagram, wherein we accept 2 inputs of each 8-bit length i.e input A(a0-a7) and input B(b0-b7), both the inputs are applied to all the operations in parallel that is all the operations are performed on the applied inputs simultaneously, after the computation the outputs of each operation are given to the MUX[4][7] respectively, based on the select lines the particular output is selected and then displayed.

An ALU (Arithmetic/Logic Unit) is the primitive unit of an adder cell. the additional features required for a system are region, power, and pace.

The most fundamental limit on mobility and portability is power dissipation and it is divided into static and dynamic energy dissipation. When the circuit is in operation, the dynamic power distribution happens, while the static power distribution becomes an issue in inert, or in shutdown mode. Three major power dispersion sources can be summarised in the digital CMOS circuits as follows:

Pavg=Pswitching + Pshortcircuit + Pleakage The initial term refers to the energy exchange segment, where C1 is the capacity of the heap, Fclk is the repetition of the clock, and α is the probability of the energy consumption progressing (the action factor). The next term is due to the immediate short circuit current ISC that occurs when the NMOS and PMOS semiconductors are turned on at the same time and conduct current directly from the power source to earth. After all, leakage currents that can arise from substrate infusion and impacts below the edge are primarily caused by increasing innovation considerations.**Td α C1Vdd/k(Vdd-Vth)$^{\alpha}$ k = transistor aspect ratio (W/L) Vth = transistor threshold voltage α = velocity saturation index which varies between 1 and 2.**

LOGICAL AND

And is the basic logical operation, the output here is high only when both the inputs are high.

4.2.1 SCHEMATIC OF 8-BIT AND

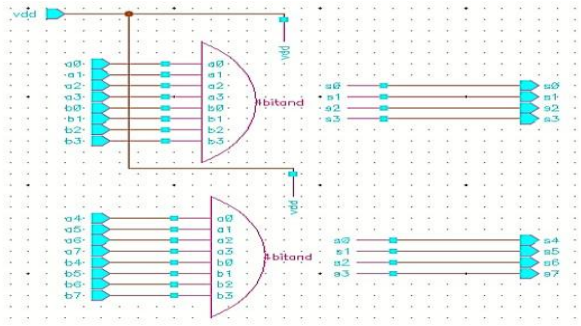

Fig 2: Schematic of 8-bit AND

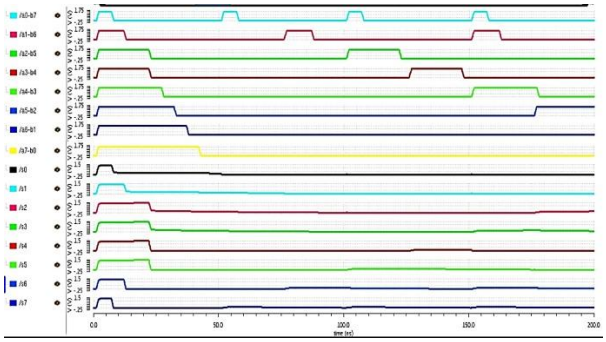

Fig 3 Waveforms of 8-Bit AND

LOGICAL OR

In logical OR operation the output is high, only when at least one input is high, this operation is almost equivalent to perform Logical addition operation.

a. SCHEMATIC OF 8-BIT OR

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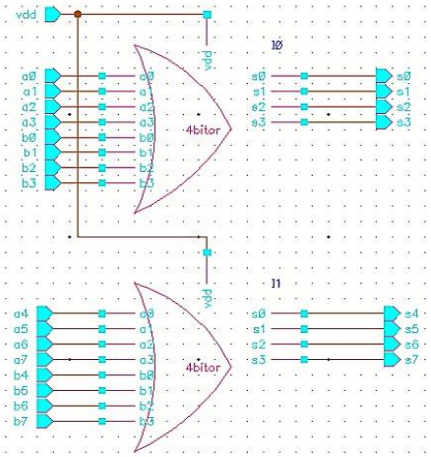

Fig 4 Schematic of 4-bit OR

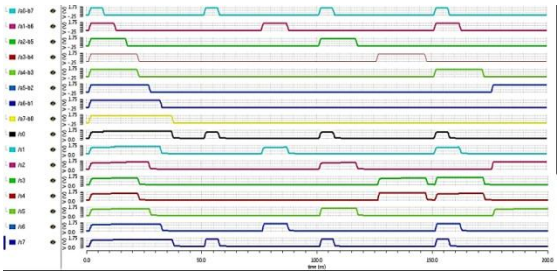

Fig 5 Waveforms of 8-bit OR

b.EXCLUSIVE OR

This operation would generate high output when both the inputs are different that is 0 and 1 or 1 and 0, the logic equation for XOR is AB'+A'B

4.4.1 SCHECMATIC OF 8-BIT XOR

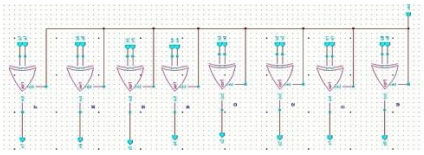

Fig 6 Schematic of 8-bit XOR operation

C.LOGICAL NAND

NAND is a universal operation, using this we can any gates in the digital circuit, NAND gate is generally described as complementing the AND gate outputs.

4.5.1 SCHECMATIC OF 8-BIT NAND

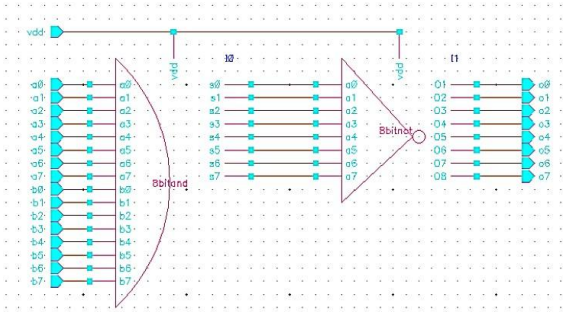

Fig 7.LOGICAL NOR

D.SCHEMATIC OF 8-BIT NOR

NOR is a universal operation, NOR operation is generally described as complementing the outputs of OR gate, that is the outputs are high only when both the inputs are LOW[3].

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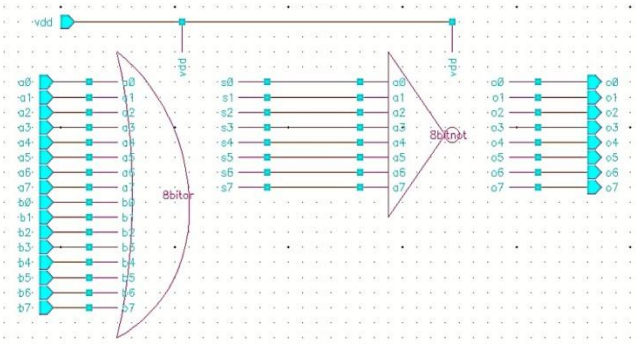


Fig 8. Schematic of 8-bit NOR

EXCLUSIVE NOR

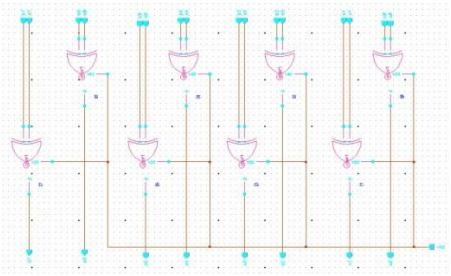


Fig 9 Schematic of 8-bit XNOR COMPARATOR:

We have designed comparator to display the greater number among the two digits.

4.14.1 SCHEMATIC OF 8-BIT COMPARATOR

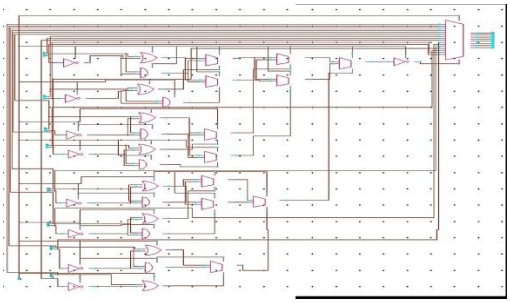
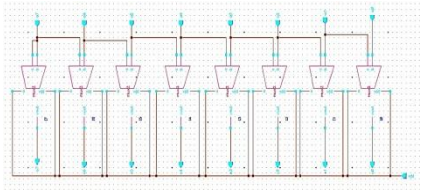


Fig 10. Schematic of comparator

ARITHMETIC RIGHT SHIFT

Here, the LSB bit is removed and all the bits are shifted by one bit by one position, the MSB bit copied into MSB-1 position, this operation is almost similar to that of performing division by 2 in decimal system

SCHEMATIC OF 8-BIT RIGHT SHIFT



Figc 11. Schematic of right shift

ARITHMETIC LEFT SHIFT:

Here, the MSB bit is removed and all the bits are shifted by one bit towards left side, and zeros are append on the LSB bit, this operation is almost similar to that of multiplication by 2 in decimal system.

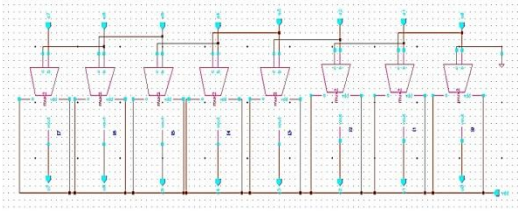


Fig 12. Schematic left shift

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13. COMPLETE ALU DESIGN

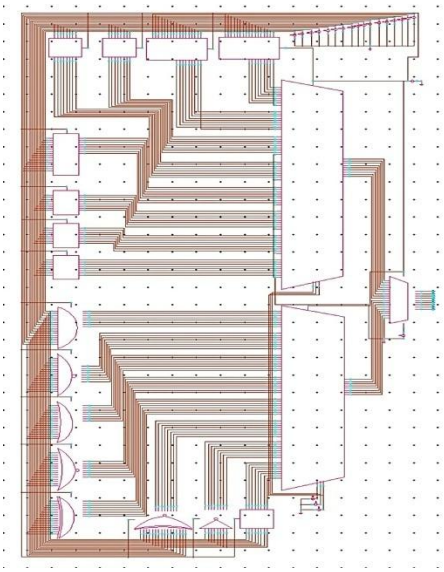

Fig 13 Schematic of 8-Bit ALU

DELAY AND POWER COMPARISSION

DELAY

The one of the important characteristics in the VLSI design is "Delay" which directly indicates the speed of operation. Generally, As technology reduces the propagation delay of the circuit also reduces. The following table depicts the comparison of delay between 90nm and 45nm technology design of 8-bit ALU. The following Figure depicts the delay calculation of sample operation in CADENCE Tool.

POWER

This is the major parameter in any circuit as it directly predicts the efficiency of the design. Now a days there are many methods and modifications are to be done in order to decrease the power consumption in the circuit. As like delay, Power also reduces from 90nm technology to 45nm technology.

The Procedure for calculation of power in CADENCE is already mentioned in the precious chapter. The following table shows the Static, dynamic and total power of the design in both the technologies.

90nm:

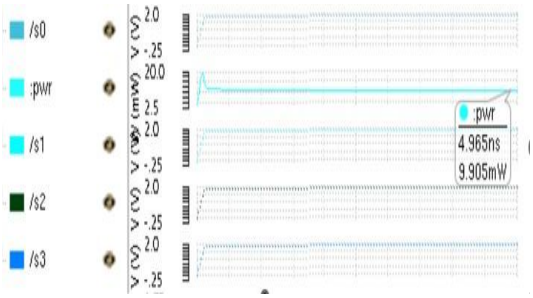

Fig 14 Static power in 90nm Technology

COMPARISION OF DELAY AND POWER IN BOTH 45nm and 90nm

Table 2. Comparison of power and delay in 45nm and 90nm

Parameter	45nm	90nm
Delay	7.44ps	17.44ps
Static power	9.428uW	9.905mW
Dynamic power	7.252uW	0.325mW
Total Power	16.68uW	10.23mW

CHAPTER 5 CONCLUSION AND FUTURE SCOPE

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5.1 CONCLUSION

We have studied the arithmetic and logical unit well. Here we have successfully implemented an 8-bit arithmetic unit that can accept 2 inputs of 8 bits each, including arithmetic operations like adder, subtraction, increment, decrement, comparator, left shift, right shift, inversion and logical operations like AND, OR, XOR , NOT, XNOR, NOR, NAND and two's complement. All the above operations have been assembled and simulated to get accurate output in both 90nm and 45nm using Cadence tool. The power and delay parameters have been calculated and we concluded that 45nm is better than 90nm because it has less delay and low power consumption.

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