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Power Efficient VLSI Architecture of 4X4 Modified Column Bypassing Multiplier

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ABSTRACT

In this work, 4X4 multiplier which has high speed and less power dissipation is mooted using CMOS VLSI circuits. The crucial parameters in chip design are area, time, power and speed. In the recent scenario, speed and power has made an important concept in Signal Processing practical applications. Various methods are available to optimize .The technique that has been discussed is a high-speed and Low power Multiplier designed based on our Column bypassing technique which is modified and primarily used for reducing the power activity in terms of switching. As this method offers more dynamic power savings, in spite of their interconnections. This paper presents a power efficient VLSI Architecture of 4x4 multiplier. The proposed design is done CMOS Technology in Cadence Virtuoso environment with working voltage supply of ±1.8v

Keywords

Braun 4X4 multiplier, bypassing coiumn multiplier, low power , High speed

Introduction

With a view to implement less delay, less power and area wise efficient and mobile design of electronics is typically impugning problem for the designers of hardware in the recent times . Portable mobile phones, cards which are with smart technology, listening aid technology such as PDAs are the example of mobile consumer electronics. The major objective of the above mentioned product are to have good operating capability and also to increase the battery working hours . Less power VLSI circuit techniques used in every hierarchy of system such as system , circuit and architecture level. More power dissipation savings can be obtained it is implemented in system level of design. Large amounts of Power dissipation can be decreased at level of design but it is at cost of delay and over headed area .Pipelining and parallel processing can also be applied at architecture and system level to reduce the power dissipation and to increase the speed . Thus, power dissipation can be lowered by the improvement in fabrication methods such as reduced feature size, very small low voltages, interconnects and insulating material with lesser dielectric constants. Threshold voltage, voltage scaling at the circuit level , sizing of Transistor, power down strategies of network restructuring and style of logic employed predominantly to gain lesser power. Some logic methods useful in the propagation delay reduction and area occupancy reduction..

Applications such as FFT and video processing and filtering are done by digital signal processors. They perform operations like MAC. Multiplication function is the main function in digital signal processors. During multiplication process, transistor undergoes high switching activity. In processor operation such as FFT , Multiplier circuit dissipates nearly thirty percent of power and utilizing fifty percent of chip area. Here by, multiplier circuit consumes more energy and also it takes more time for computation. Different techniques are applied internally and externally in the previous schemes, in order to get energy efficient designs of multiplier. Schemes which are external are linked to the only input data attributes,

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where in as an internal scheme originally deals with the technology, system architecture and circuits.

Literature Review

Multiplication is one of the important arithmetic operation which is done by the usual DSP functions including FFT modules and FIR filters. The power consumption is reduced in the multiplier which can reduce a large amount of power dissipation in the present electronics world. The m bit number A and B can be multiplied and defined as follows

$$P = A \times B = \sum_{i=0}^{i-1} \sum_{j=0}^{j-1} \left(\left(A_i B_j \right) 2^{(i+j)} \right)$$

Where in the P represents the partial product of the multiplication operation.

		A =	a_3	a_2	a_1	a_0	
		(×) B=	b_3	b_2	b_1	b_0	
			a_3b_0	a_2b_0	a_1b_0	a_0b_0	
		a_3b_1	a_2b_1	a_1b_1	a_0b_1		
	a_3b_2	a_2b_2	a_1b_2	a_0b_2			
a_3b_3	a_2b_3	a_1b_3	a_0b_3				
P_7	P_6	P_5	P_4	P_3	P_2	P_1	P_0

Figure 1: Multiplication Process

In the applications of DSP, Multiplication based on array multiplier is a reasonable option because of small circuit and high speed. It depends on regular shift and add operations. Its circuit is set by various stages of full adder cells and AND gates. The circuit might consist of either carry save adders (CSAs) or ripple carry adders (RCAs). For multiplication using RCAs multiplier requires three number of adders and in the worst case it takes 2N+1 adders delay. Multiplier using Carry save adders requires 3N adders to design multiplication so that in the worst case it takes N + 2 adders delay.

Existing Model:

The two numbers which is having n bit that too unsigned can be multiplied by using array parallel multiplier where A is the multiplicand and B is the multiplier.

This multiplier operating in parallel is adapted to implement the multiplication which is unsigned. The Braun multiplier architecture is made up of AND gates array and 3 bit adder circuit. To implement multiplier require 3 bit adders and AND gates. Braun multiplier delay

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will be proportional to the delay present in the full adders and also the delay present in the final adder which is a ripple carry adder. The dynamic power dissipation of the multiplier resulting from the switching activities can be reduced via bypassing techniques By employing Column bypassing Row bypassing and reversible logic techniques, the dynamic power due to switching activity can be minimised.

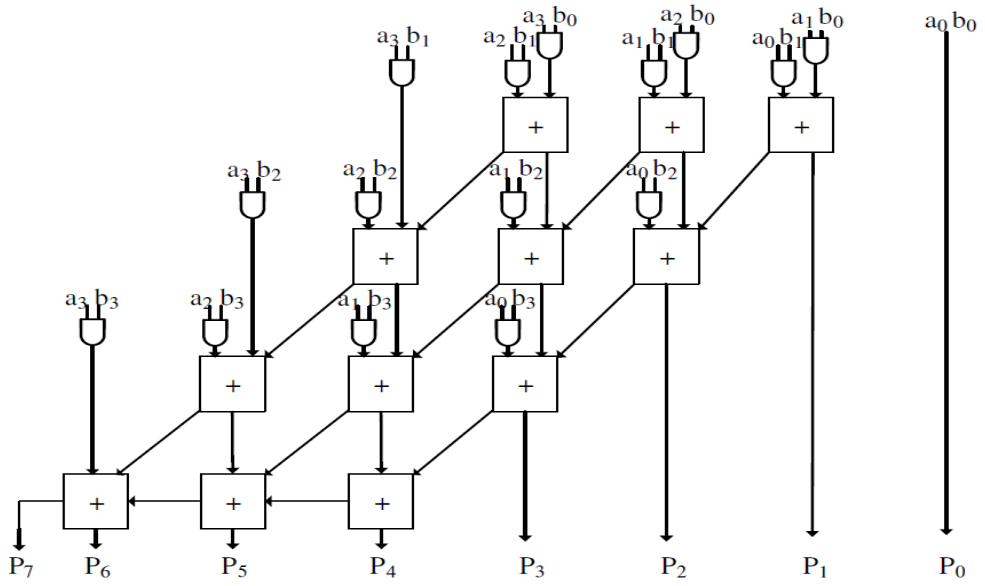

Figure 2: Braun Multiplier

Braun multiplier execute very well for the operands which are unsigned and which are lesser than bits of size 16 in the aspect of the power, speed and circuit area. However it is quite elementary structure when compared to the other complex multipliers. Array multiplier could be implemented and power could be analysed for different full adders like CMOS normal full adder, 17 transistor full adder, 15 transistor full adder and SERF 11 transistor full adder and from the comparison the power optimized multiplier will be found out. Four different full adders are used for analysis.

Proposed Modified Column bypassing multiplier:

At the input of the adder cells where we could find the Tri-state buffers and which are thrusted to decrease the transitions of switching if and only when the adder cells are avoided or bypassed. However, Multiplexer is forced to opt sum output sum without avoiding when the bypassing is used. The operation of addition in (i-1)t h column could be avoided for the (i)t h if and only if when the same identical bit is zero in the multiplicand . This operation can be designed by not activating the adder which can be disabled using buffer which can be controlled by ai multiplier bit

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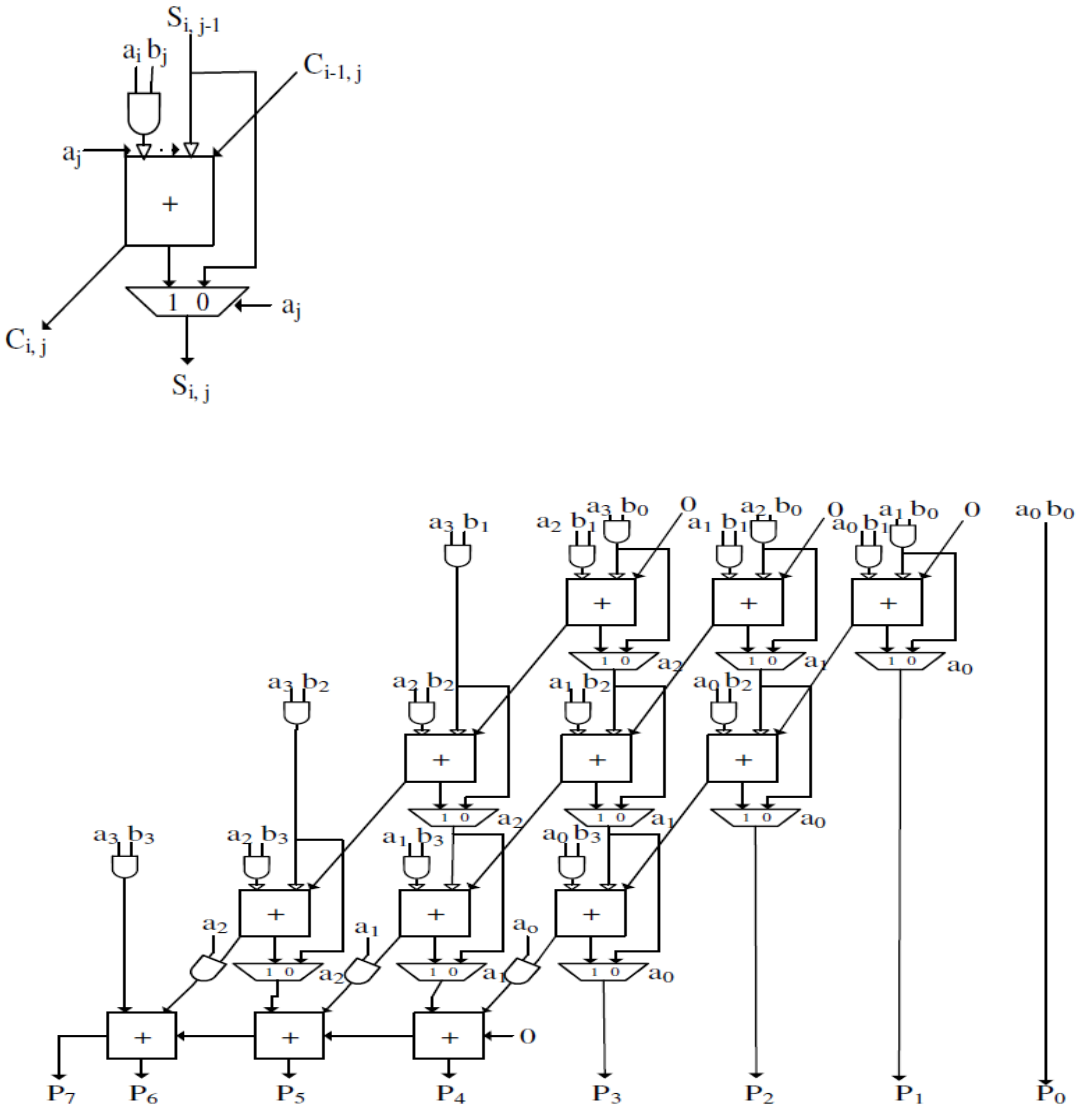

Figure 3: Proposed Modified Column Bypassing Multiplier

In any stage, all the inputs of the partial product in the column does not influence the carry.That is the reason why here one 2:1 multiplexer is reduced which has not been required at the output of carry. Therefore, The multiplier based on Column bypassing is simpler to design when it is compared to multiplier by Row Bypassing . In Column Bypassing multiplier, each of the adder is added with tri-state buffers which are only to get the partial product inputs. Tri-state buffer does not need at the input side of the carry in the case of multiplier which is column bypassed. At the output side, Only one 2:1 multiplexer is connected and of to change in between normal path and bypassed path. Carry is not affected in the multiplier which is column bypassed.

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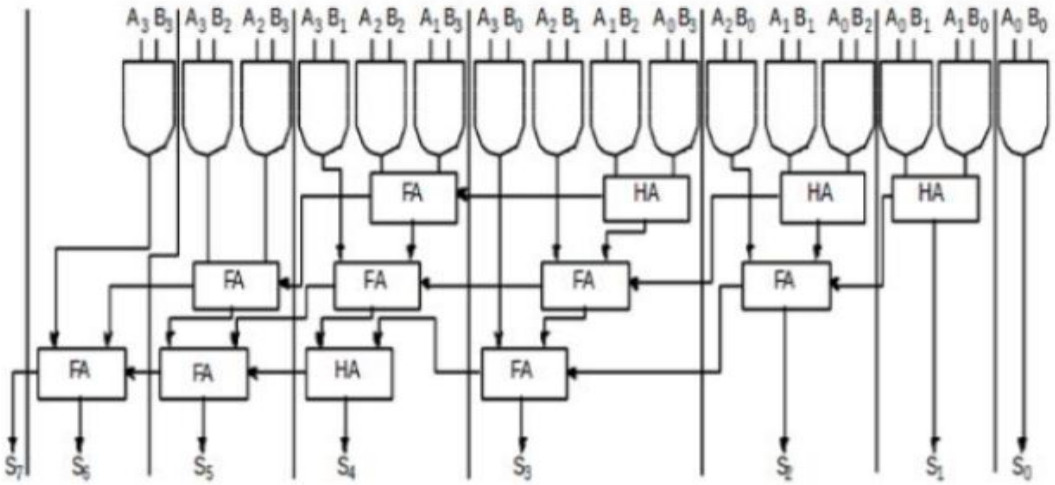

Figure 4: Column bypassing multiplier

Simulated Results and Discussions:

Mooted multiplier design and normal multiplier working performance comparison is done using delay and energy consumed. The design is simulated in cadence virtuoso schematic editor Environment. The proposed multiplier design results are congruence with regular design. This proposed structure is for design 16-bit and 8-bit multipliers.

Following figure denotes the schematic of the commonly known as the braun multiplier:

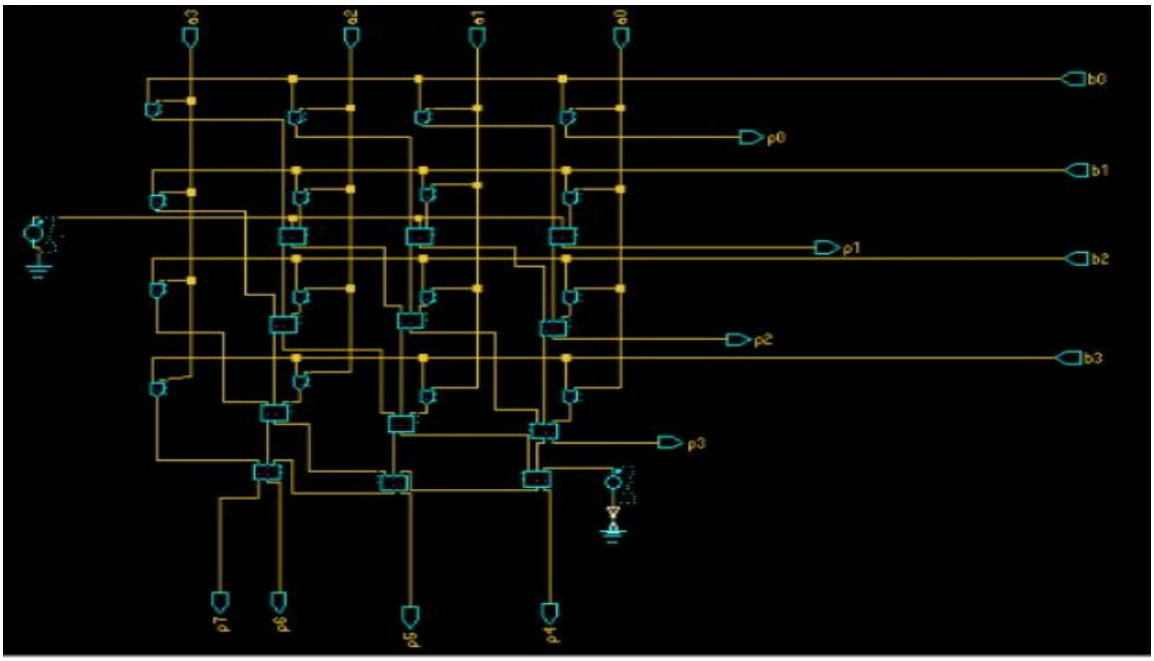

Figure 5 : Existing parallel array multiplier(Braun Multiplier)

The following figure denotes the schematic of the in cadence tool:

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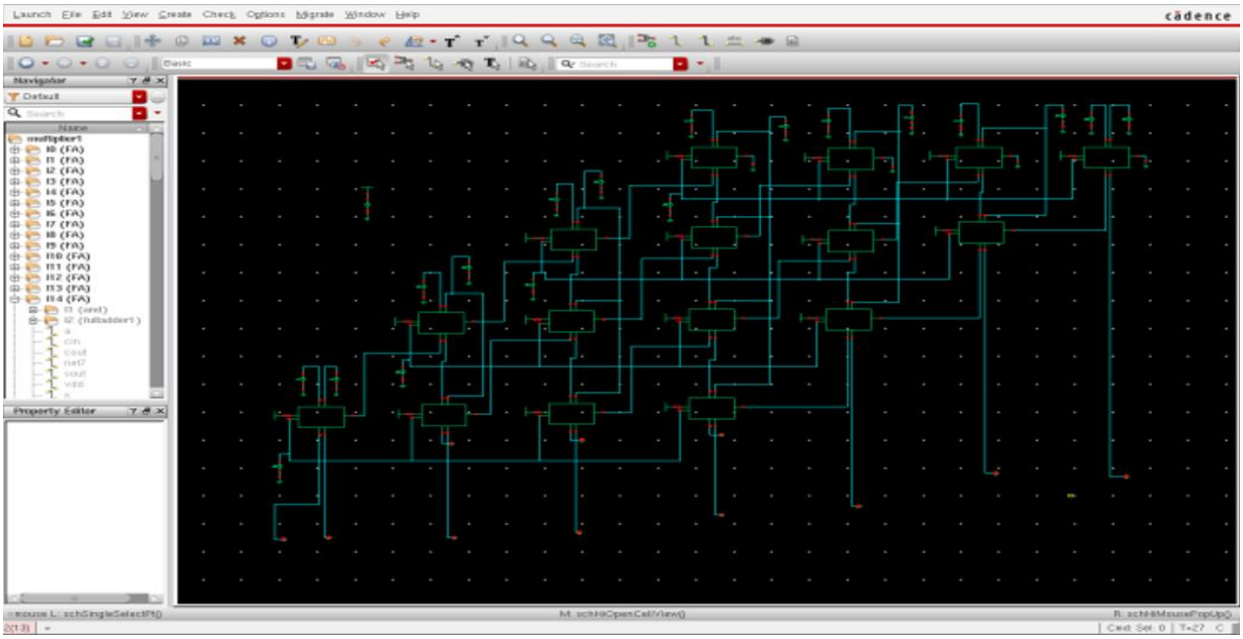

Figure 6: proposed modified column bypassing multiplier

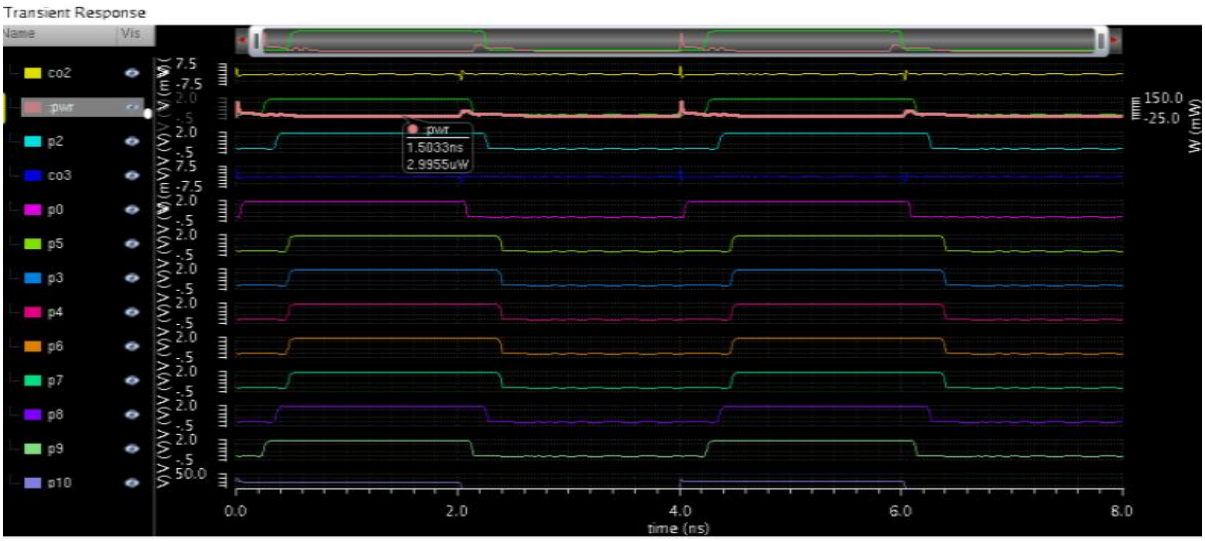

Figure 7: Output of the Proposed Modified Column bypassing multiplier

Table 1: Power and delay Analysis of Multipliers

Parameters	Braun Multiplier	coloumn bypassing Multiplier
Power Supply	1.8v	1.8v
Power Consumption	7.99microwatt	2.99microwatt
Delay	1.9ns	1.3ns

In regular Design, the consumed energy is 11.34nwatts, dissipation close to 7.99µwatts where as the delay equal to 1.9ns. In the design which is mooted, dissipation of power in circuit is found to be 2.4nwatts , power consumption is found to be 2.99µwatts and delay is equal to

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1.3ns. Last, the proposed design results are found to be superior when comparing to the Conventional design.

Conclusion:

A high speed and low power multiplier utilising a changed c bypassing column structure is mooted. The mooted experiment gives amazing result in power consumption reduction and delay reduction The Simulated design indicates that multiplier which is mooted design provides a decreasing in power and also less requirement for area .

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