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Design of Adaptive FIR based Algorithm for Reducing noise Feedback Signal on Digital Hearing Aid System

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Abstract

This paper presents adaptive filtering algorithm for processing noise signal which are present in ambient environment for digital hearing aid system. Conventional hearing aid system suffers from noise signal due to imbalance in the signal boost which degrades the original speech signal and reduce the capability of the hearing signals in noise environment. This can be reduced by utilizing adaptive filtering techniques in the FIR filter bank. However this method is very unstable since their weights are modified frequently. The proposed model design is written in Verilog and realized using Synopsys design compiler using 90 nm technology. The model is realized for 32, 64 and 128 adaptive filters coefficient lengths and are compared with traditional pipelined DA based adaptive FIR filter. The model achieves42.61% lesser area and 29.42% lesser ADP along65.13% power reduction and 41% of PDP compared with the traditional designs.

Keywords:FLR adaptive filter, Hearing Aid, Adaptive beam former, optimal filter.

1. INTRODUCTION

The presence of noise in the ambient environment degrades the hearing capability for those with hearing impairment. This will be severe with prolonged exposure to those harsh environment. In [1], reported that the people having hearing impairment faces much difficulty in hearing in adverse environment when compared with quiet pleasant environment due to ambient noise. Even person with mild hearing loss has good understanding of speech in quiet environment in normal environment suffer poor hearing at noise environment. In general the behavior of the noise around the subject vary dynamically [3] from time to time. This includes wind noise, human speech noise and other mechanical and electrical sources. Hence there is a necessity to develop hearing aid which can adapt to the environment. The use of digital signal processors in the hearing aid system was coined in last decades [4] and later extensive works on digital hearing aid system is developed to enhance the hearing quality [5-6]. Lots of studies on acoustic in the digital hearing aid system has been carried [7-8] in recent years to make the hearing aid dynamically adapting according to the environment. A novel variable filter-bank (VFB) comprising of multiple filter bank channels each embedded reconfigurable gains and band edges, is depicted [9] which gives better flexibility. A digital finite impulse response (FIR) filter bank is demonstrated by [10] which is having efficient computation capability. A non-uniform cosine modulated filter bank is proposed [11] for hearing aid application.

In this paper, a novel filter bank based on reconfigurable FIR filter is utilized to minimize the noise in the ambient environment. The filter model utilizes reduced number of filter

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coefficients to enhance the computation complexity of the system. In addition to that, the filter coefficients are adaptively tuned with respect to the ambient environment.

2. PROPOSED ARCHITECTURE

The general architecture of the modern digital filter is depicted in Fig. 1 given below. The model comprises of an input audio receiver sensor which are then preprocessed by means of analog low pass noise filter. An analog to digital converter having significant resolution is utilized for conversion. It is the processed by means of proposed digital filter bank having a feedback path from the output signal. The signal is then amplified and are given to output side.

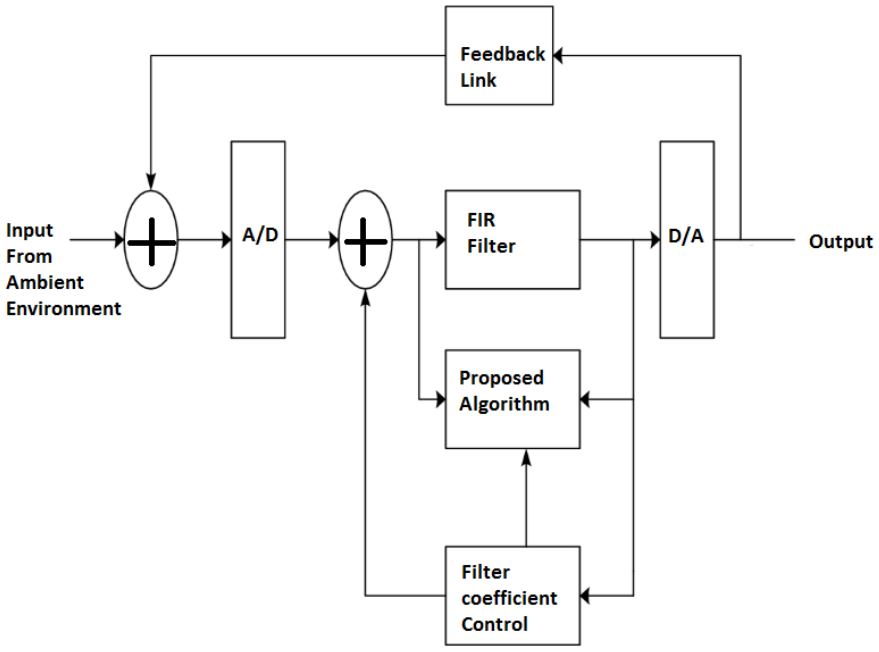

Fig. 1. General Architecture

2.1 Adaptive algorithm

In this algorithm, the output of the filter is computed at each stage along with feedback signal taken form the output. The input to the filter is taken as $I(n)$ which is given as

$$I(n) = [I(n), I(n-1) \dots \dots \dots . . I(n-N+1)]^T \quad (1)$$

where$I(n)$ is signal input at an instant time 'n'. The signal output corresponding to the model is given by $O(n)$ which is given below

$$O(n) = I^T(n)C(n) \quad (2)$$

Where filter coefficient is represented by $C(n)$ and is derived from

$$C(n) = [C_0(n), C_1(n)C_2(n) \dots \dots \dots . . C(N-1)(n))]^T \quad (3)$$

The filter coefficients $C(n)$are tuned based on the noise signal$e(n) = O(n) - I(n)$present in the ambient environment which is based on LMS algorithm whose weights are adjusted by step size μ.

$$C(n+1) = C(n) + \mu e(n)I(n) \quad (4)$$

2.2 FIR Filter Coefficient selection

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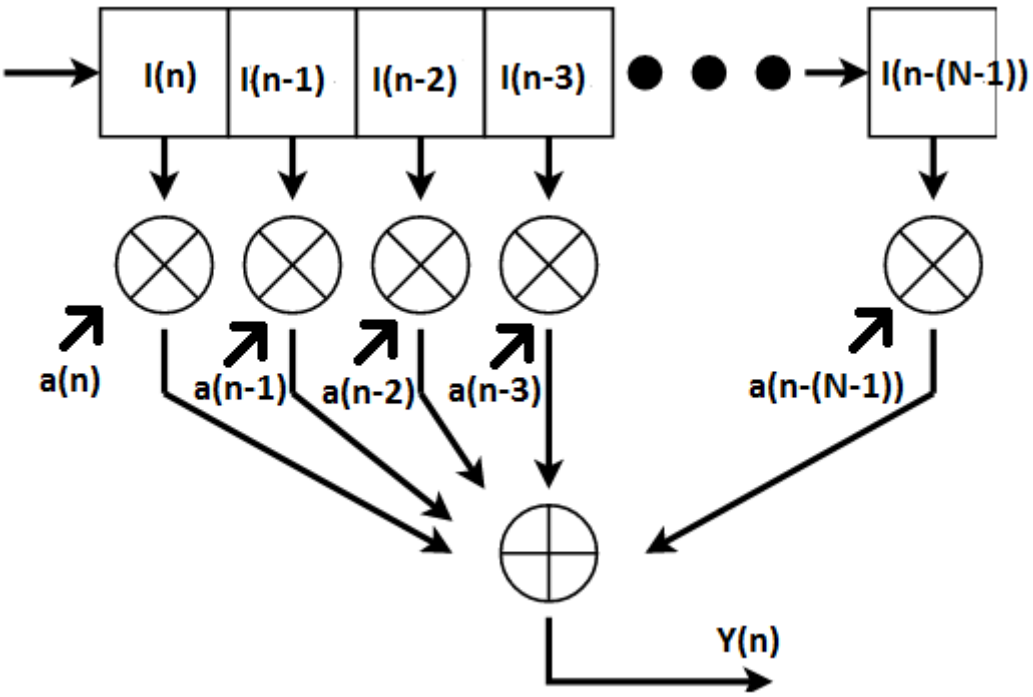

Fig. 2. FIR Filter Bank

The filter coefficients are selected based on the input signal $I(n)$ and are given by

$$O = \sum_{n=0}^{N} C_n I_n \quad (5)$$

Where I_n corresponds to input data and C_n corresponds to filter coefficients. For a given filter having a length of N which is 2's complement of binary number,

$$I_n = -b_{n0} - \sum_{n=1}^{N-1} b_{kn} 2^{-n} \quad (6)$$

$$O = \sum_{n=0}^{N} C_n(-b_{n0} - \sum_{n=1}^{N-1} b_{kn} 2^{-n}) \quad (7)$$

$$O = \sum_{k=1}^{K-1}[\sum_{n=1}^{N} C_n b_{kn}]2^{-n} + \sum_{n=1}^{N-1} C_n(-b_{n0}) \quad (8)$$

3. RESULTS AND DISCUSSIONS

The proposed model is compared with existing model and are given in Table 1. The model design is written in Verilog and realizedusing Synopsys design compiler using 90 nm technology. The performance metrics area, power and delay is inferred from the synthesis result. The proposed model is realized for 32, 64 and 128 adaptive filters coefficient lengths as given below. From the table 1, whencompared with traditional pipelined DA based adaptive FIR filter (Levitt 1987), it is inferred that the proposed modelachieves42.61% lesser area and 29.42% lesser ADP along65.13% power reduction and 41% of PDP compared with the traditional designsas depicted in given table.

Table 1 Synthesis of ASIC based on 90 nm technology

Design	Filter length K	Area (sq. µm)	Throughput (per µs)	MSP ms	Power (mW)	PDP (mWXns)	ADP (sq.µm × ns)
Allred et al. (2005)	32	143377.33	50.6	24.05	1.5249	36.6738	3441048
	64	267146.33	46	27.24	2.9062	79.1648	7277057
	128	537053.63	40	29.78	5.311	158.16158	15993438
Guo and	32	107520.8	77	25.8	0.7555	13.45	2774016

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DeBrunner (2011)	64	209082	71	31.8	1.4598	46.42	6648807
	128	416418	64	35.8	2.7315	97.7877	14907770.49
Park and Meher (2013)	32	88719	141.04	7.09	2.917	20.68153	629617.71
	64	177460	120.33	8.31	5.834	48.48054	1474692.6
	128	364820	104.167	9.6	11.67	112.032	3502272
Proposed design	32	74450.25	53.01	9.7225	1.0942	16.7753825	808713.8567
	64	148469.5	46.0825	11.0275	2.141375	29.253648	1638246.309
	128	113384.75	61.30175	4.1725	3.64675	33.1783825	2065944.855

Figures 3 and 4 shows the power delay product and area delay product graphs.

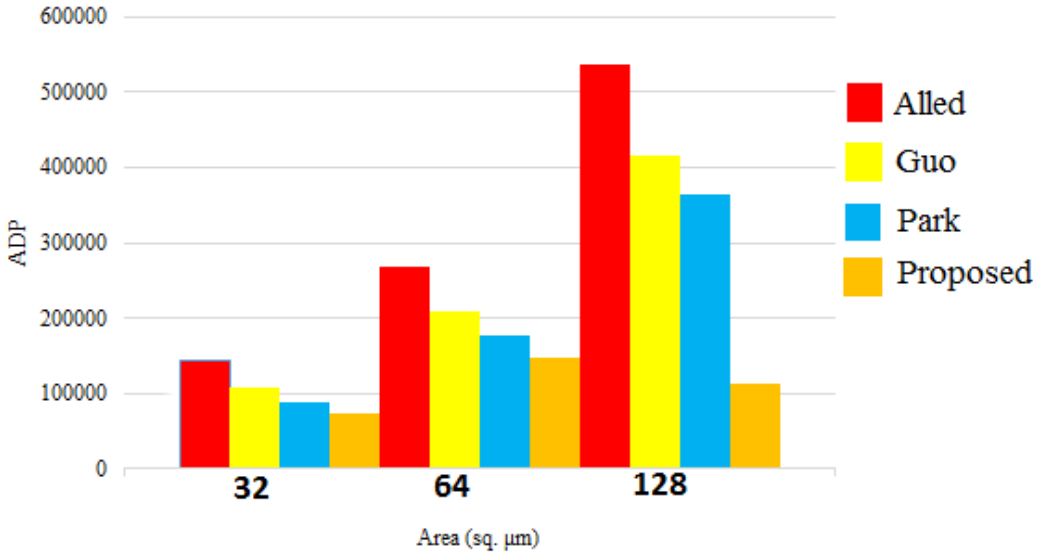

Fig. 3. Area delay product (ADP)

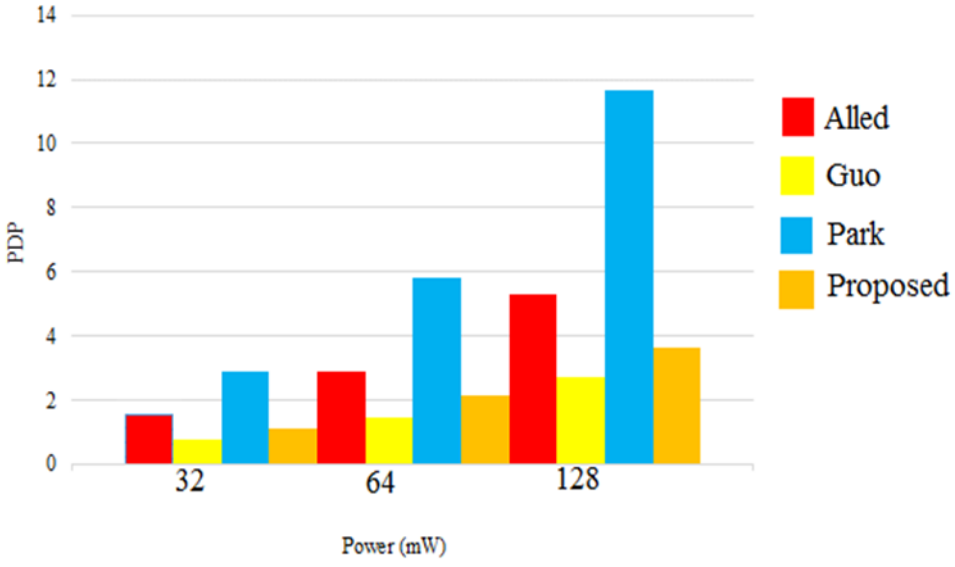

Fig. 4. Power delay product (ADP)

4. CONCLUSION

In this paper, a novel FIR based filtering for noise cancellation in the ambient environment is proposed. The proposed model design is written in Verilog and realized using Synopsys design compiler using 90 nm technology. The model is realized for 32, 64

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and 128 adaptive filters coefficient lengths and are compared with traditional pipelined DA based adaptive FIR filter. The model achieves lesser area and ADP alongwith power reduction compared with the traditional designs.

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