Annals of R.S.C.B., ISSN:1583-6258, Vol. 25, Issue 3, 2021, Pages. 2102 - 2110
Received 16 February 2021; Accepted 08 March 2021.

Simulation and Performance Analysis of Electrical properties of Nano Scale Surrounding Gate MOSFET

Aditya Agarwal[1], R L Sharma[2], Prashant Mani[3]

[1,2]Department of ECE, Noida International University , Noida, Uttar Pradesh, INDIA
[3]Department of Electronics & Communication Engineering, SRM Institute of Science and Technology, Modinagar, Uttar Pradesh, INDIA

Abstract: In this paper we propose an improved nano scaled Surrounding gate MOSFET utilizing Silvaco TCAD software. When the channel length of the bulk planer MOSFET is scaling down, a planer MOSFET experiences short channel effects and reduce the device performance. The different parameter like drain characteristics are extracted for Surrounding gate MOSFET. The analytical results are verified with the help of 3D TCAD Silvaco device Simulator. The results represent the greater performance is acquired for surrounding gate MOSFET. Surrounding Gate MOSFET current drivability is high as compared with bulk planer MOSFET. Surrounding gate MOSFET attains great possibility to become a future device as bulk planer MOSFETs for creation of upcoming generation with low power, high speed devices.

Keywords: Surrounding gate MOSFET, DIBL, short channel effects.

Introduction: In present fast technological advancements and scaling down device dimensions up to deep sub-micron level over the last decades have made this realizable to achieve high speed integrated circuits with less power consumption. When shrink down dimensions of the device up to deep micro meter region, some effects like threshold voltage issue, DIBL (drain induced barrier lowering) and quantum mechanical effects be predominant and major effects on device performance. However, shrinking down the device width will reduce the gate controllability and current driving capability by disturbing the voltage distribution. These effects degrade the device performance and develop challenge for further down scaling the MOS technology [1]. Today's technology demands the reduction of threshold voltage for very high speed devices. The device reaches to minimize channel width and channel length for the bulk planer MOSFET attains enhance packing density [4, 5].

Surrounding Gate MOSFET (SG MOSFET) is a unique device which provides considerably surprising results in the technologically application areas. The solution for overcome the scaling limitations of bulk planer MOS devices and to achieve enhance packing density for upcoming device analysis. Changes in device geometry from its planer traditional shape may improve device performance and reduce the limitations. The device shows less power dissipation, increase energy efficiency and increase speed of operation [2].

SG MOSFET is characterized under non planer device in which channel lies in vertical direction. In SG MOSFET gate is surrounded with silicon pillars and decreases MOS transistor area. SGMOSFET shows the better control on Short channel effects, can be shrink down for minimum length of channel and oxide thickness [3, 5].

SG MOSFET produces extra advantages as improved current and enhanced transconductance. SG MOSFET device geometry is different with bulk planer MOSFET [1]. Here physical device design enhances the Gate control over channel voltage that improves threshold affection, increase packing density and enhances short channel immunity [5, 10].

Device Structure: SG MOSFET is a device where gate electrode is surrounded from all sides, where gate is in cylindric style structure. The source and drain areas lies between two edges of MOS. Now increase

Annals of R.S.C.B., ISSN:1583-6258, Vol. 25, Issue 3, 2021, Pages. 2102 - 2110
Received 16 February 2021; Accepted 08 March 2021.

the gate control over the channel conduction that impacted decrease in drain voltage inside the channel too [5]. SG MOSFET produces best control over the gate voltage when formation of channel achieved. The Surrounding Gate MOSFET increases current drivability more than bulk planer MOSFET [6, 20].

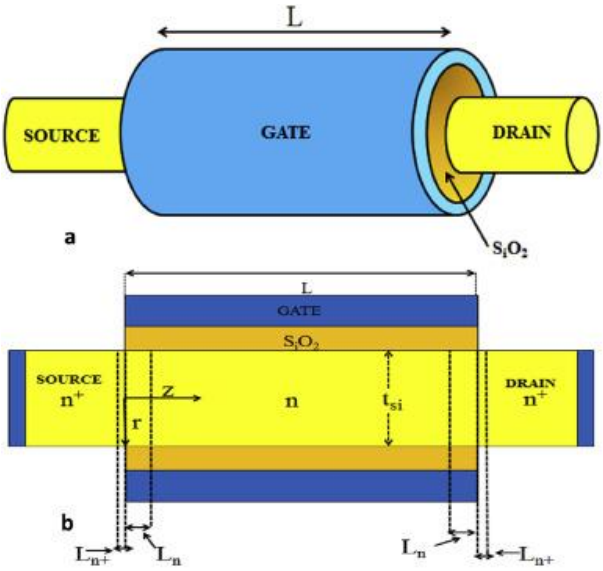

Fig.1:Surrounding Gate (SG) MOSFET

The produced device structure is as the characteristics L = 40nm, R = 15nm, C_{ox} = 1.3, μ = 0.48, D = 0.10, S = .05.
The Surrounding Gate MOSFET required lesser on voltage instead of bulk planer MOSFET. Surrounding gate MOSFET device performance ratio I_{on}/I_{off} is high as compared to bulk planer MOS which means the leakage current will be very small and it also reduces power dissipation.

DEVICE MODELING: Here we obtained the simulated $I_{DS}(V_{GS}, V_{DS})$ characteristics of SG MOSFET. We explored the drain current performance for various regions of the device operations in different areas [5].

For drain current calculation, the drain current is evaluated in drain and source ends and obtained an expression. The inversion region drain current is expressed as [5, 10]

$$I_{ds}(z) = 2\pi R Q_n(z) \frac{\mu(dV(z)/dz)}{1+(1/E_{sat})(dV(z)/dz)} \qquad (1)$$

Where, R is radius and device width is 2πR. V(z) = channel voltage in z direction, dV(z)/dz = electric field in z direction. Critical field is $E_{sat}= 2V_{sat}/\mu$, saturation velocity is V_{sat} and mobility isμ.

$$\mu = \frac{\mu_0}{\sqrt{(1+[N_A/(N_{ref}+(N_A/S))])}} \qquad (2)$$

Mobility of electron is μ_0= 677cm^2/Vs. N_{ref} = 3x10^{22} m^{-3}, S = 350

N_A is p – type doping concentration [5]. Surface charge density is $Q_n(z)$ at any point z is expressed as

Annals of R.S.C.B., ISSN:1583-6258, Vol. 25, Issue 3, 2021, Pages. 2102 - 2110
Received 16 February 2021; Accepted 08 March 2021.

$$Q_n(z) = C_{ox}(V_{gs} - V_{th} - V(z)) \quad (3)$$

Oxide capacitance - gate (C_{ox}) is,

$$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}} \quad (4)$$

$$\varepsilon_{ox} = \varepsilon_o \varepsilon \quad (5)$$

The drain current eq. (linear region), simplified eq. (1) and substitute the above equations in equation no. (1) and integrating the eq. is obtained as:

$$I_{ds} = \frac{2\pi R \mu C_{ox}(V_{gs} - V_{th} - (\frac{V_{ds}}{2}))}{L(\frac{1}{V_{ds}} + \frac{1}{LE})} \quad (6)$$

The drain current eq. (saturation region) is given by [1]

$$I_{dsat} = 2\pi R V_{sat} Q_{nsat} \quad (7)$$

Where, I_{dsat} is drain current (saturation) and is Q_{nsat} is inversion charge obtained on $V_{ds} = V_{dsat}$ is expressed as

$$Q_{nsat} = C_{ox}(V_{gs} - V_{th} - V_{dsat}) \quad (8)$$

Put Q_{nsat} value in equation (7) given by

$$I_{dsat} = 2\pi R V_{sat} C_{ox}(V_{gs} - V_{th} - V_{dsat}) \quad (9)$$

Threshold voltage V_{th}, Drain saturation voltage V_{dsat} obtained by

$$V_{dsat} = \frac{(V_{gs} - V_{th})}{1 + (V_{gs} - V_{th})/LE} \quad (10)$$

When channel length (device) decreases, effects (short channel) like DIBL, punch through effects take into the account then these impacts the action of the future device. As a consequence of DIBL the short channeled device's charge inside the channel is controlled by the drain voltage instead of gate voltage [3, 6]. So DIBL effects can incorporate in our SG MOSFET structure [10, 11].

The drain current (replacing by threshold voltage -V_{th}) in equation (6) by V_{th}"

Annals of R.S.C.B., ISSN:1583-6258, Vol. 25, Issue 3, 2021, Pages. 2102 - 2110
Received 16 February 2021; Accepted 08 March 2021.

$$I_{ds} = \frac{2\pi R\mu C_{ox}[V_{gs} - V_{th''} - (\frac{V_{ds}}{2})]}{L(\frac{1}{V_{ds}} + \frac{1}{LE})} \quad (11)$$

We know that V_{ds} is more than V_{dsat}, means pinch off point act close to source and difference in voltages ($V_{ds} - V_{dsat}$) is dropped with length 1_d. This provides results in produces drain current enhancement [3].

Here we obtain channel length (modulation) effects saturation current with term replacing L by (L - l_d) [8, 11]

$$I_{dsat} = \frac{2\pi R\mu C_{ox}[V_{gs} - V_{th} - (\frac{V_{dsat}}{2})]}{\frac{(L - l_d)}{V_{dsat}}(1 + (\frac{V_{ds}}{(L - l_d)E}))} \quad (12)$$

Where l_d = velocity saturation length and V_{sat} = saturation velocity is in the saturation region [5].

Result and Discussion: SG MOSFET operation is showed in fig. 1. Here we investigated simulated and analytical region operations with different applied potential at gate [5]. Here voltage (drain to source - V_{ds}) varies within the range 0 to 5V, figure shows when voltage (drain to source - V_{ds}) increases simulated drain current increases rapidly as compared to analytical drain current values. When gate voltage (V_{gs}) increases, then the amount of charge carriers emits from source side also increases [5, 9]. DIBL of SG MOSFET also observed.

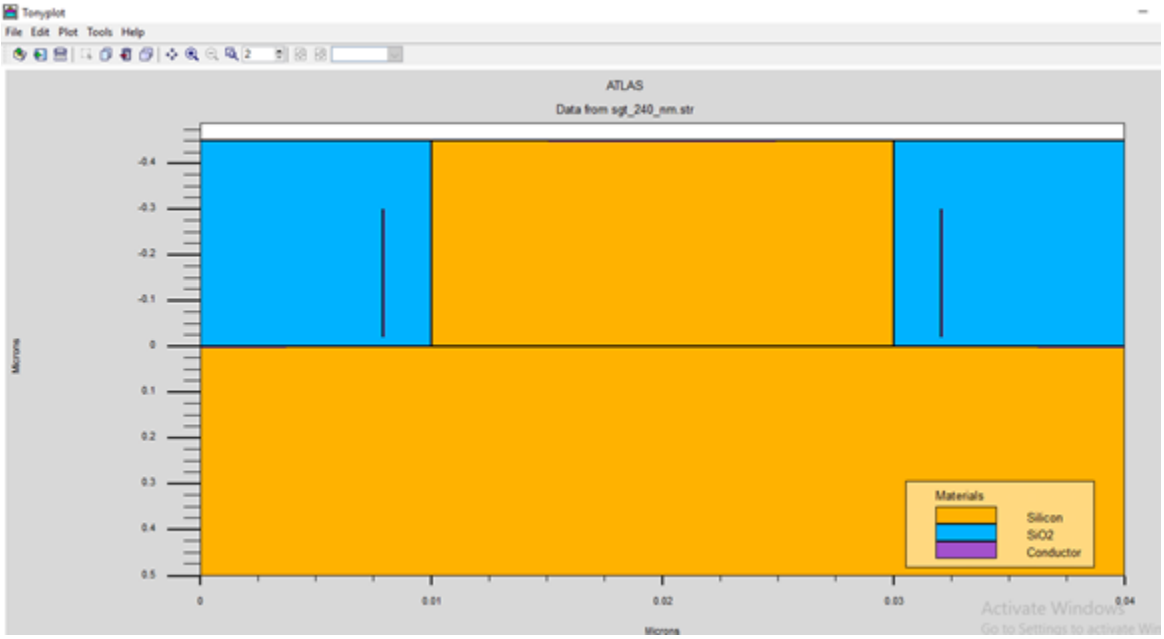

Fig.2: Device structure of Surrounding Gate MOSFET

Annals of R.S.C.B., ISSN:1583-6258, Vol. 25, Issue 3, 2021, Pages. 2102 - 2110
Received 16 February 2021; Accepted 08 March 2021.

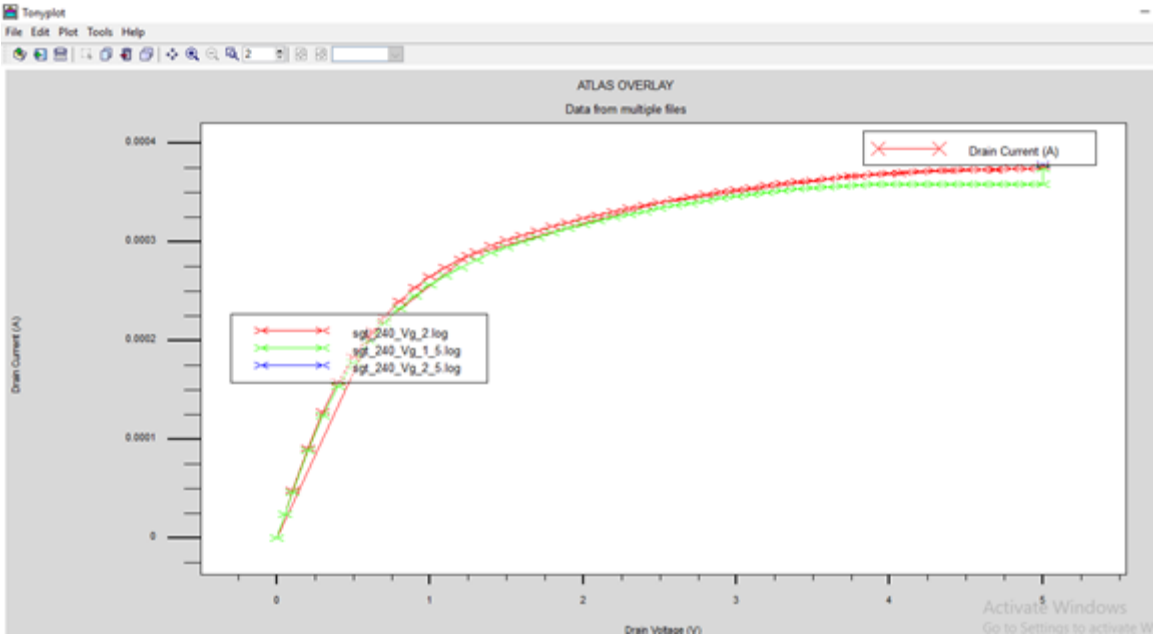

Fig.3:Simulated $I_D$vs V_{DS} characteristic of Surrounding Gate MOSFET

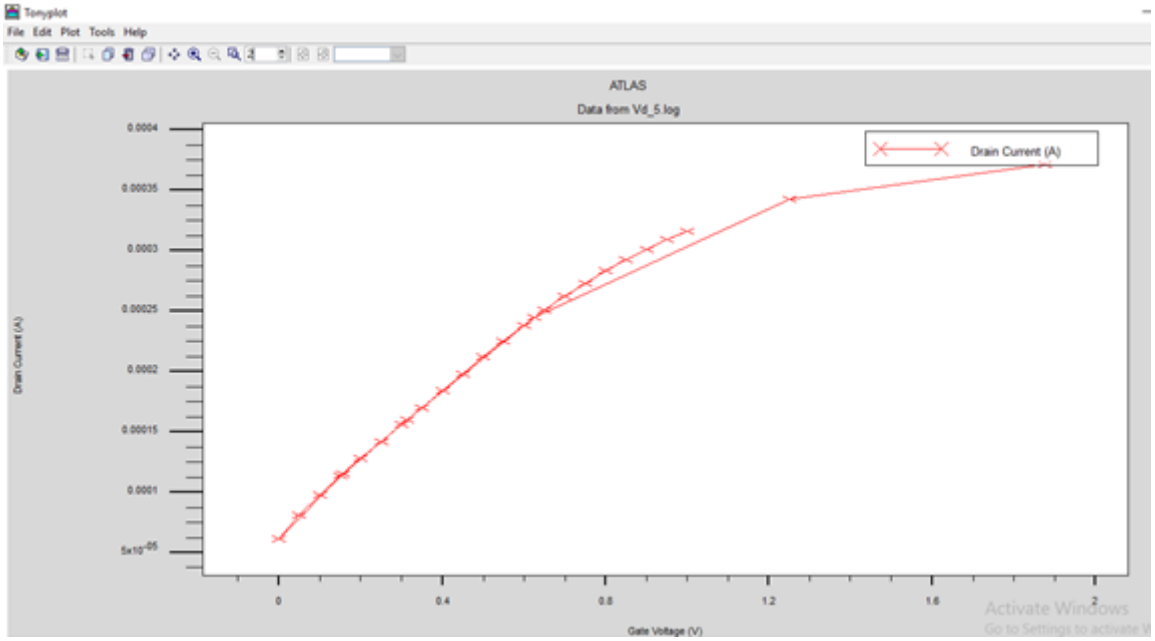

Fig.4: $I_D$vs V_{GS} characteristic of Surrounding Gate MOSFET

Annals of R.S.C.B., ISSN:1583-6258, Vol. 25, Issue 3, 2021, Pages. 2102 - 2110
Received 16 February 2021; Accepted 08 March 2021.

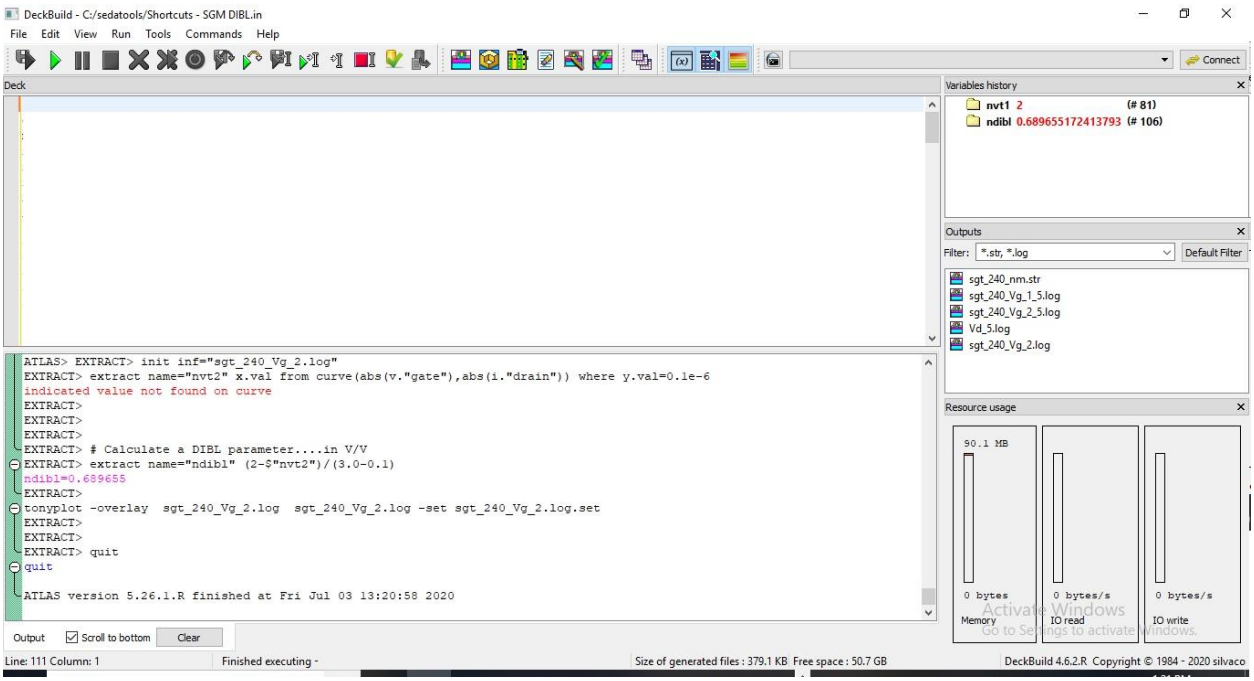

Fig.5: DIBL of Surrounding Gate MOSFET

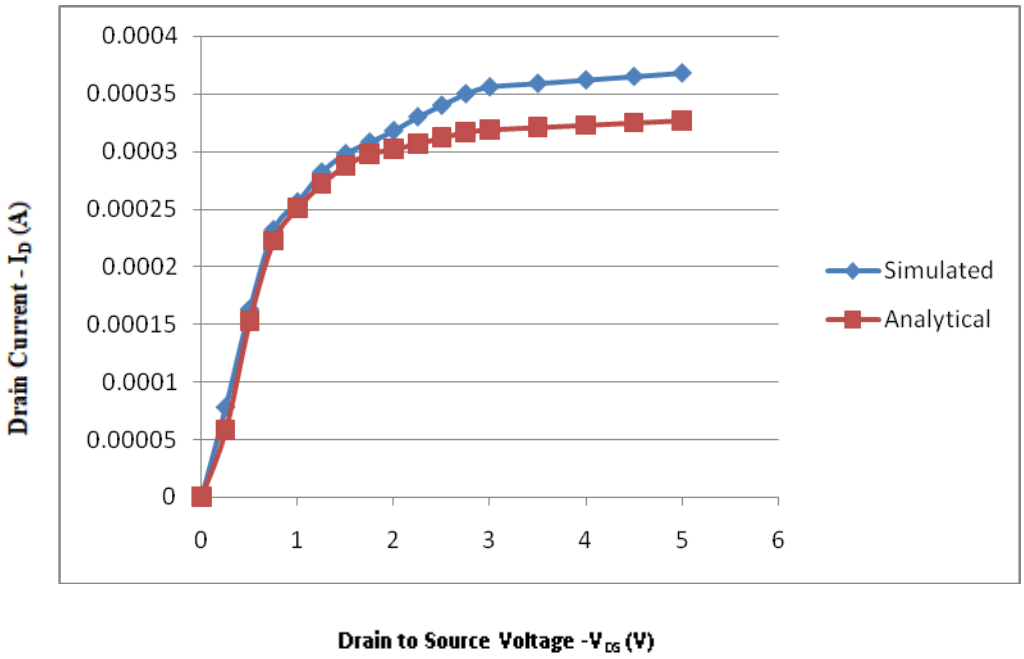

Fig.6: I_D – V_{DS} characteristic of Surrounding Gate MOSFETat V_{GS} = 1.5V

Annals of R.S.C.B., ISSN:1583-6258, Vol. 25, Issue 3, 2021, Pages. 2102 - 2110
Received 16 February 2021; Accepted 08 March 2021.

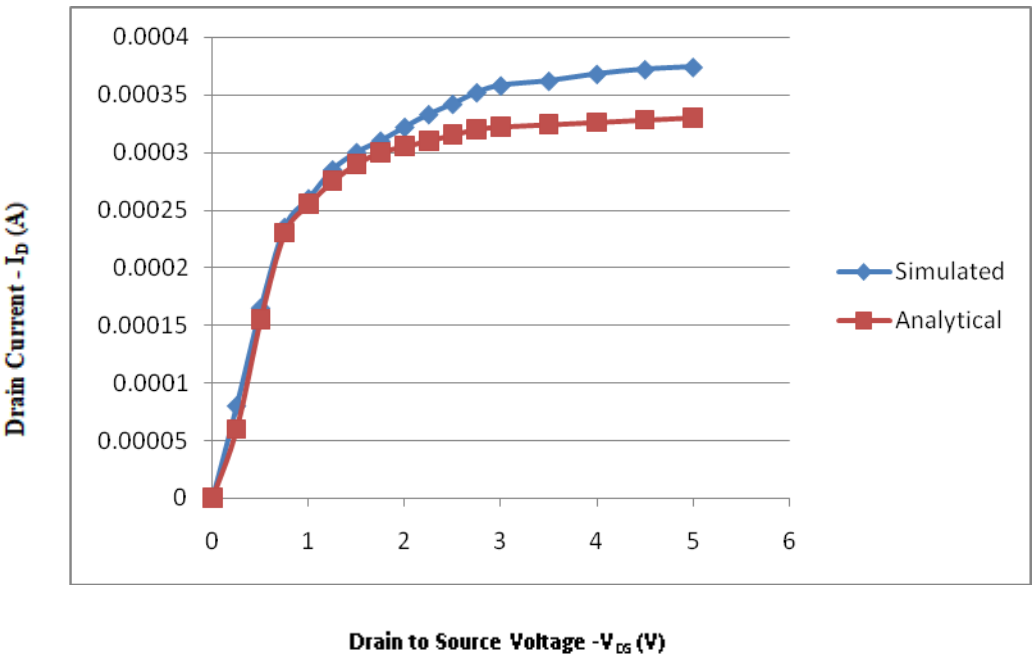

Fig.7: I_D – V_{DS} characteristic of Surrounding Gate MOSFET at V_{GS} = 2V

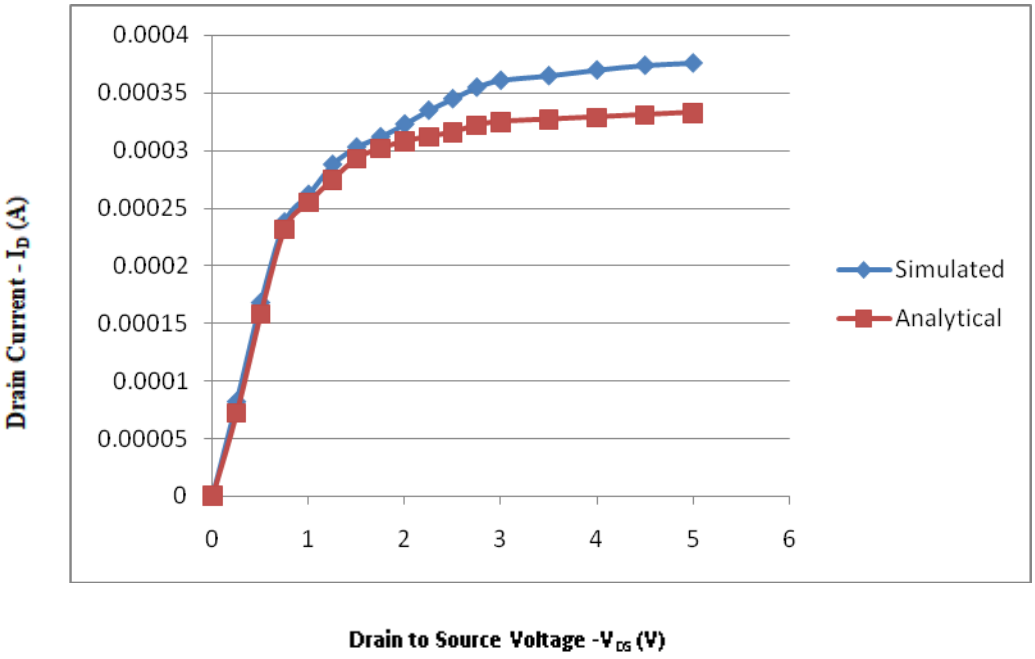

Fig.8: I_D – V_{DS} characteristic of Surrounding Gate MOSFETat V_{GS} = 2.5V

Annals of R.S.C.B., ISSN:1583-6258, Vol. 25, Issue 3, 2021, Pages. 2102 - 2110
Received 16 February 2021; Accepted 08 March 2021.

Conclusion: The Surrounding gate (SG) MOSFET behavior investigated in different operating conditions. Surrounding Gate MOSFET has been adopted for developing future devices, which minimize the power dissipation and reduce the occupied area. Here channel is surrounded by the gate so we receive better electrical control compare to conventional MOSFETs.

REFERENCES

[1] H. Kaur, S. Kabra, S. Halder, R. S. Gupta, " An analytical drain current model for graded channel cylindrical/surrounded gate MOSFET, Microelectronics Journal, Vol. 38, Issue 3, March 2007, pp:352-359.

[2] B. Jena, B. S. Ramakrishna, S. Dash, G. P. Mishra, "Canoical surrounding gate MOSFET: a possibility in gate all around family", IOP Publishing, Advances in Natural Sciences: Nanoscience and Nanotechnology, 7 (2016).

[3] N. Gupta, J. B. Patel, A. K. Raghav, "A study of traditional and Surrounding Gate MOSFET using TCAD simulations", International Journal of science & Technology, Vol. 9, Issue 47, Oct. 2016, pp: 1 – 5.

[4] D. Jimenez, B. Iniguez , J. Sune, L. F. Marshal. J. Pallares, J. Roig, D. Flores, "Continuous Analytic I-V model for Surrounding gate MOSFETs", IEEE Electron Device letters, Vol. 25, Issue. 8, August 2004.

[5] A. Agarwal, R. L. Sharma, P. Mani, "Analytical Modeling Electrical Conduction of Nano Scaled Surrounding - Gate MOSFET", IEEE International Conference on Micro-Electronics and Telecommunication Engineering,
DOI 10.1109/ICMETE.2018.00078, pp: 331-334.

[6] M. Subrahmanyam, J. M. Kumar, "Recessed source concept in nanoscale vertical surrounding gate (VSG) MOSFETs for controlling short channel effects, Physica E: Low-dimensional systems and Nanostructures" , Vol. 41, Issue 4, 2009, pp: 671-676.

[7] B. Cousin, M. Reyboz, O. Rozeau, M. A. Jaud, T. Ernst.,J. Jomaah., "A unified short channel compact model for cylindrical surrounded-gate MOSFET",Elsevier -Solid state Electronics, Vol. 56, Issue 1, 2012, pp: 40-46.

[8] Sabina, Kushwaha A. K., "Dual material Gate all around Fully Depleted SOI MOSFET with strained Si/Ge channel", International Journal of Engineering Research and Applications, Vol. 3, Issue 4, Aug 2013, pp: 2335 - 2340.

[9] Yu B., Lu W.Y., Lu H., Taur Y., "Analytical charge model for surrounding gate MOSFETs", IEEE Transactions on Electron Devices, Vol. 54, Issue. 3, March 2007,pp: 492-496.

[10] A. Kranti, S. Halder, R. S.Gupta, "Analytical model for threshold voltage and IV characteristics of fully depleted short channel cylindrical/surrounding gate MOSFET", Microelectronics Engineering Elsevier, Vol. 56, 2001, pp: 241-259.

[11] N. D. Arora, R. Rios, C. L. Huang, K. Raol, "PCIM: A physical based continuous short channel IGFET model for circuit simulation", IEEE Transaction on Electron Devices, Vol. 41, Issue 6, June 1994, pp: 988-997.

[12] V. M. Srivastava, K. S.Yadav,G. Singh, "Explicit Model of Cylindrical Surrounding Double-Gate MOSFET" WSEAS Transactions on Circuits and Systems, Vol. 12, Issue 3, 2013.

[13] P. SuveethaDhanaselvam, N. B. Balamurugan, N. Basheer Ahmad, " A charge control model of Surrounding Gate MOSFET", International Journal Engineering of Compute science, Vol. 2, Issue 3, March 2013, pp: 777-780.

[14] B. Yu., H. Lu., "Analytical charge model for Surrounding Gat MOSFETs", IEEE Transactions of Electron Devices, Vol. 54, Issue 3, March 2007, pp: 492 – 496.

Annals of R.S.C.B., ISSN:1583-6258, Vol. 25, Issue 3, 2021, Pages. 2102 - 2110
Received 16 February 2021; Accepted 08 March 2021.

[15] H. Sood, V. M. Srivastava, G. Singh, " Advanced MOSFET technologies for next generation communication systems- perspective and challenges: A review", Journal of Engineering Science and Technology Review, Vol. 1, Issue 3, 2018, pp: 180-195.
[16] A. Agarwal, R. L. Sharma, P. Mani, "A study of characterization of Surrounding Gate MOSFET", VSRD Journal of Technical and Non-Technical research, Vol. 9, Issue 1, January 2018, pp:67-70.
[17] C. P. Auth, J. D. Plummer, " A simple model for threshold voltage of Surrounding Gate MOSFETs", IEEE Transactions on Electron Devices, Vol. 45, Isssue 45, Nov. 1998, pp: 2381 – 2383.
[18] J. H. Park, J. Young Song, J. P. Kim, S. W. Kim, J. G. Yun, B. G. Park, "Fabrication of highly scaled silicon nanowire gate all-around metal-oxide-semiconductor field effect transistors by using self-aligned local channel V-gate by optical lithography process", IOP Science - Japanese Journal of Applied Physics, Vol. 49, No. 8R, August 2010, 084203.
[19] T. Mukaiyama, K. Saito, H. Ishikuro, M. Takamiya, T. Saraya, T. Hiramoto, "Fabrication of gate all around MOSFET by silicon anisotropic etching technique", Solid State Electronics, Vol. 42, Issue 7-8, August 1998, pp: 1623-1626.
[20] A. Agarwal, R. L. Sharma, P. Mani, "A study of characterization of Surrounding Gate MOSFET", VSRD Journal of Technical and Non-Technical research, Vol. 9, Issue 1, January 2018, pp:67-70.
[21] P. Ghosh.,S. Halder, R. S. Gupta, Gupta M., " An analytical drain current model for material engineered cylindrical/surrounding gate MOSFET", Elsevier -Microelectronics Journal, Vol. 43, Issue 1, January 2012, pp:17-24.
[22]H. Takato, K. Sunouchi, N. Okabe, a. Nitayama, K. Hieda, F. Horiguchi, F. Masuoka, " Impact of Surrounding Gate Transistor (SGT) for ultra-high density LSI's", IEEE Transactions on Electron Devices, Vol. 38, Issue 3, March 1991, pp: 573 – 578.