

Performance Investigation of Electrical Parameters of OTFT for Different Dielectric Materials

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ABSTRACT

Gate dielectrics have a significant impact on transistor performance. The selection of dielectric material is critical in the design of organic thin film transistor (OTFT). This study examines the effect of variation in dielectric material on the performance of OTFT with organic semiconductor layer of binaphth[2,3-b:2',3'-f]thieno[3,2-b]thiophene (DNFT) using ATLAS simulation. Electrical features including maximum drain current (I_{dmax}), Current on-off ratio (I_{on}/I_{off}), threshold voltage (V_{th}), and transconductance (g_{max}) differ drastically depending on the dielectric material. The change in electrical parameters is mostly caused by the gate insulating capacitance of the dielectric layer. Using variety of gate insulators, including SiO_2 , HfO_2 , Al_2O_3 and Si_3N_4 , 2D numerical simulations of OTFT are performed. Study confirms that high current on-off ratio (I_{on}/I_{off}) with HfO_2 dielectric makes it suitable for various fast switching applications. Organic transistors have a promising future with memory devices, inverters, DNA sensors and RFID tags among its many possibilities.

Keywords:-Organic;Flexible;Dielectric

Introduction

Organic thin film transistors (OTFTs) have shown promise in a range of applications, including flexible displays, memory devices, and RFID tag components [1]. The Organic semiconductor devices are low cost, low processing temperature with flexibility than inorganic electronics. Plastic, paper, and even cloth can be used as flexible, elastic substrates for electronic circuits [2,3,4]. Improved organic device performance, such as maximum drain current, trans conductance, on-off current ratio and threshold voltage (V_{th}) voltage is a major concern for expanding the use of real-time commercial applications like memory device and biosensing applications [5]. Semiconductor layer, dielectric material, dielectric interface, trap states and device geometry influence the electrical characteristics of OTFT [6]. This

research uses a variety of insulators to examine how they alter the value of electrical parameters of the OTFT [7,8]. In addition to physics-based OTFT characteristics, the dielectric material influences electrical aspects such as current on-off ratio (I_{on}/I_{off}), drain current and threshold voltage (V_{th}) voltage. As the dielectric constant decreases, off current increases due to a change in bulk current. Practically with a greater dielectric constant, switching and memory devices require a lower off current [9,10]. One way to improve OTFT performance is to choose the right insulating material during the manufacturing process. The performance parameters of the devices are affected due to traps at the interface. In memory and display circuits, a high on-off current ratio is also one of the important parameters [11].

Literature Review

In literature, dielectric effect on performance parameter of PANI based OTFT has already been presented and discussed [12]. Effect of bilayer dielectric have significant impact on the performance parameters of OTFT [13]. The performance analysis with different dielectric is also done on dual gate pentacene based OTFT [8]. It has been seen that high K dielectric shows, better performance for digital applications [9]. The effect of dielectric material on the performance of OTFT having different organic active materials such as pentacene, P3HT and DNTT has been proven in a number of studies. There hasn't been an investigation related to the performance of electrical parameters of DNTT-based OTFTs with different gate insulating materials. All electrical parameters for various insulators utilized in DNTT-based OTFT are examined using Silvaco's ATLAS two-dimensional numerical device simulator.

This paper has four sections. The simulation theory is given in next section. Subsequently, the results are discussed and the last section presents the principal observation from the investigation's findings.

Simulation Theory

The geometry of OTFT under consideration, and the parameters employed in simulation technique, are described in this section. The device simulator by Silvaco ATLAS is used to execute two-dimensional simulation studies. The simulator employs drift diffusion equations, Poisson's equation, and continuity equations, to model flow of charge carriers. As illustrated in Figure 1, OTFT using DNTT as an active material is simulated with a variety of dielectric. To get a large capacitance, the thickness of dielectric material is 5.3 nm which is extremely thin. Circuits run at a low voltage due to their enormous capacitance. The channel width of OTFT is 25 micro meter and length of channel is 0.8 micro meters.

The structural features of all the devices are listed in Table 1.

In this simulation, the poole-frenkel mobility model is used to represent hopping of charge transfer carrier in organic semiconductor like pentacene and DNTT [14]. In the pool-frenkel mobility model, charged particles move due to higher activation of trapped charge carriers in the fields. The Poole-frenkel mobility model [2], is used because DNTT exhibits substantial good hole mobility, which can be stated mathematically as equation (1)

$$\mu(E) = \mu_0 \exp\left[-\frac{\Delta E_a}{kT} + \left(\frac{\beta}{kT} - \gamma\right)\sqrt{E}\right] \quad (1)$$

zero electric field mobility is given by μ_0 , $\mu(E)$ is electric field mobility, β is the poole-frankel factor, ΔE_a is zero field activation, field intensity is denoted by E, γ is fitting parameter, T denotes temperature and K denotes boltzmann constant.

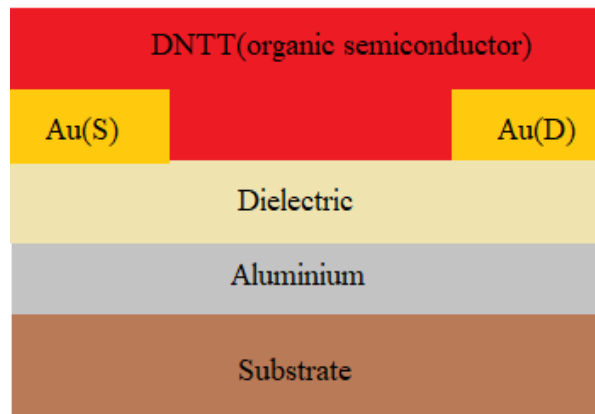


Figure 1. Structure of OTFT

Table 1. Design Parameter of OTFT

Device Parameter	Value of parameter
Thickness of Insulator	5.3nm
Thickness of DNTT	25nm
Gate material Thickness	30nm
Thickness of gold contacts	30nm
Channel width in OTFT (W)	25 μm
Channel length in OTFT(L)	0.8 μm

Result and Discussions

SiO₂, HfO₂, Al₂O₃ and Si₃N₄ are among the popular gate dielectrics used to imitate OTFT. The researched OTFT model's transfer characteristics with various dielectrics are shown in Figure 2 (a). By extending the plots in Figure 2 (b), the threshold voltage (V_{th}) is computed. Even though the simulation settings and device dimensions are the same, the threshold voltage (V_{th}) differs for different insulators due to changes in dielectric capacitance. The electrical performance parameters such as threshold voltage (V_{th}), drain current on-off ratio and transconductance (g_{max}) are compared in Table II for OTFTs with gate insulators. The electrical properties of various gate insulators tends to change due to differences in dielectric constant and surface instabilities at the semiconductor dielectric interface [15]. HfO₂ dielectric material has the highest on-off current ratio among the four insulators-based OTFTs due to its high permittivity. The transconductance (g_{max}) of HfO₂ increases dramatically as the dielectric changes. Figure 2(c) shows that, transconductance (g_{max}) keeps increasing as dielectric constant increases, finally maximize for HfO₂ dielectric, due to the large field intensity induced across the OTFT. On-off current ratio increases as dielectric constant increases. On-off ratio for HfO₂ is calculated as 10^9 that is highest in all dielectric used in research, as shown in Figure 2(a).

Table 2.Comparative study of performance parameters of OTFT using various dielectrics

Performance parameter	SiO ₂	Al ₂ O ₃	Si ₃ N ₄	HfO ₂
Maximum Transconductance(g_{max})	7.50×10^{-6} S	1.18×10^{-5} S	1.7×10^{-5} S	4.04×10^{-5} S
Threshold Voltage(V_{th})	-0.5V	-0.64	-0.75 V	-0.85 V
Maximum Drain current(I_{dmax})	9.56×10^{-6} A	1.57×10^{-5} A	2.31×10^{-5} A	5.66×10^{-5} A
Current on-off ratio(I_{on}/I_{off})	6.08×10^7	1.66×10^8	3.40×10^8	1.41×10^9

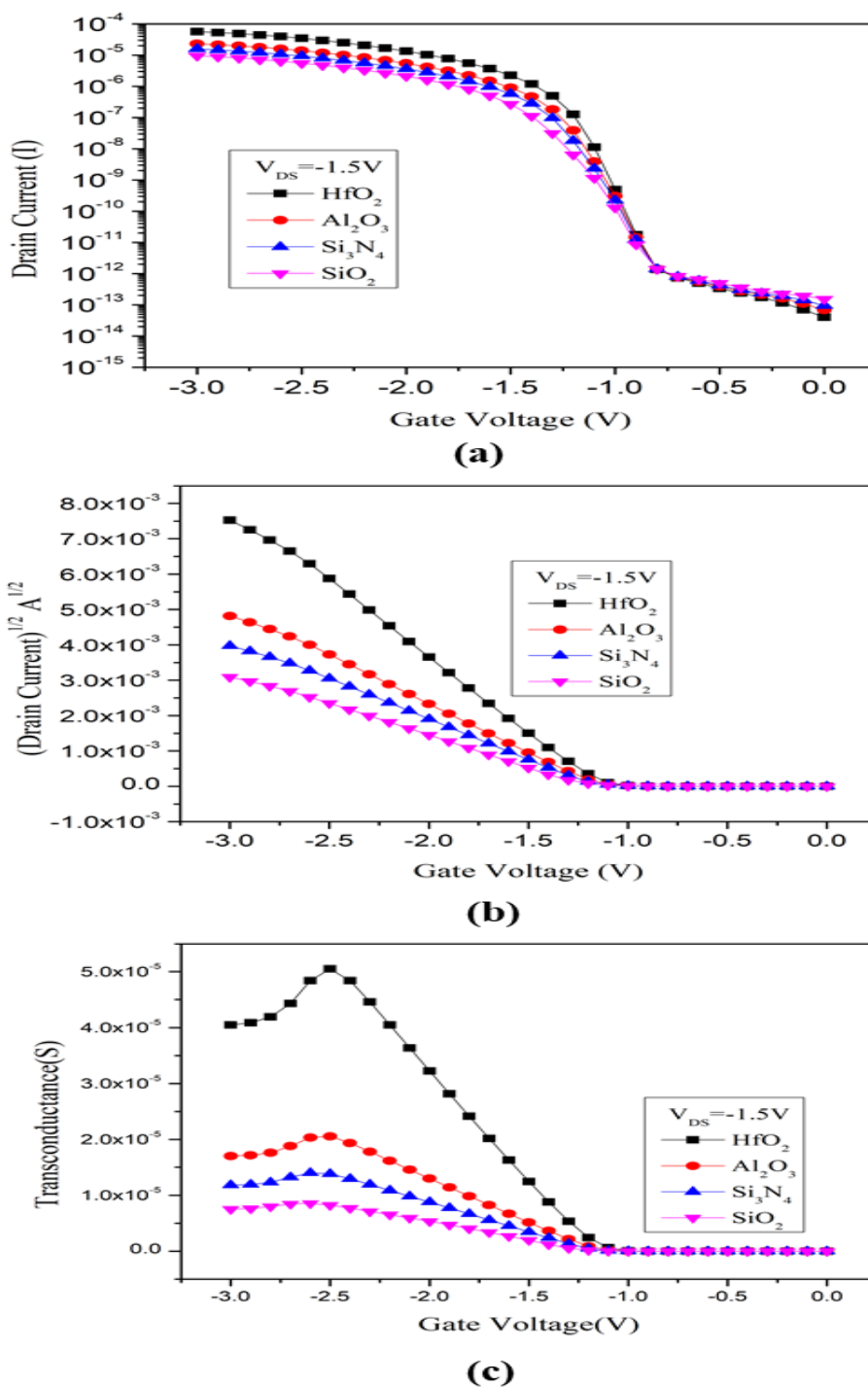


Figure 2. (a) OTFT transfer characteristics (I_d v/s V_{gs}) using different insulators (b) (square root of I_d v/s V_{gs}) characteristic of OTFT using different insulators (c) Transconductance v/s Gate voltage (V_{gs}) plot for different insulators

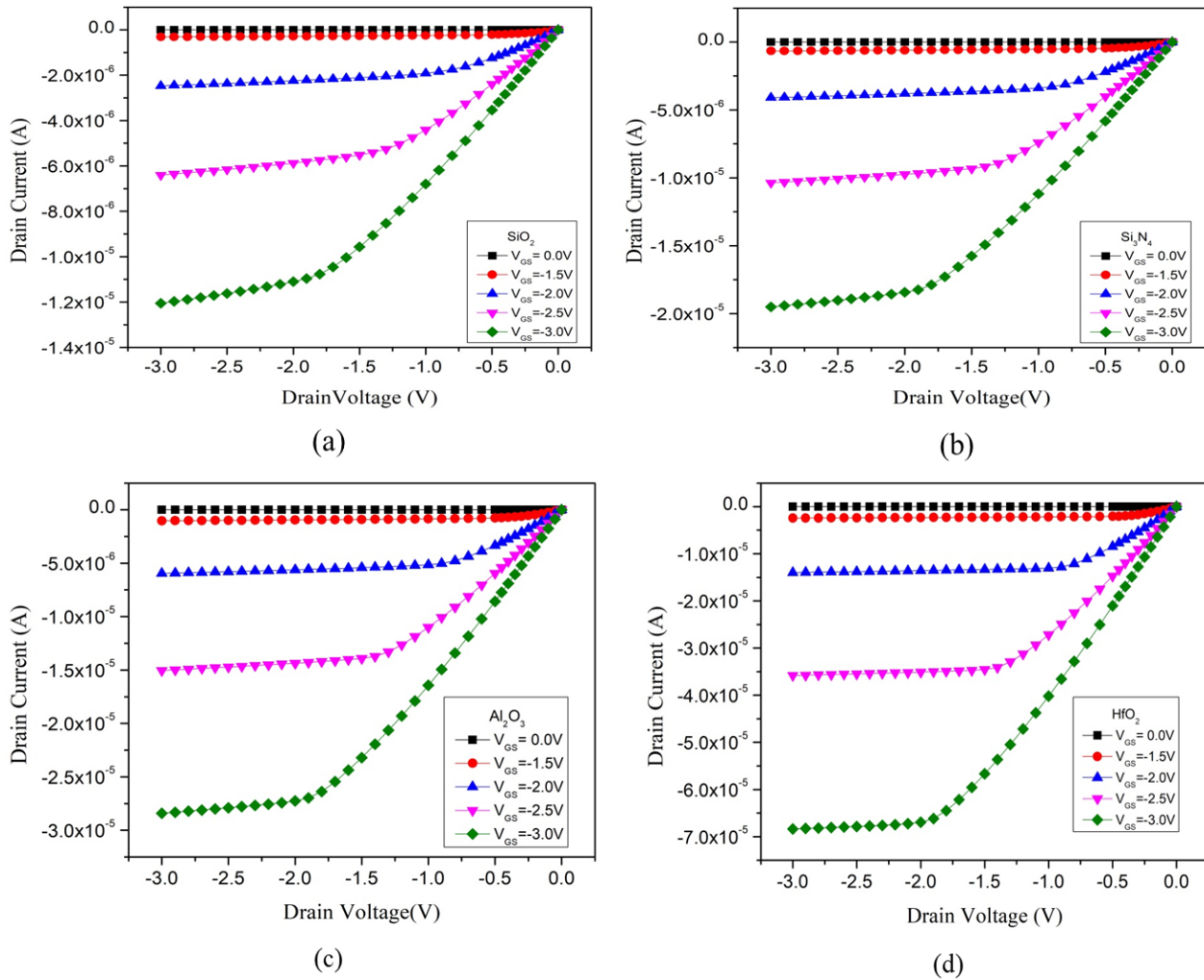


Figure 3. OTFT drain characteristics (I_d v/s V_{ds}) for various dielectric (a) SiO_2 (b) Si_3N_4 (c) Al_2O_3 (d) HfO_2

Keeping all dimensional parameters constant for all simulated devices, when compared to other dielectrics, hafnium oxide (HfO_2) performs well, with a current on-off ratio of 10^9 and transconductance (g_{\max}) of $4.04 \times 10^{-5} \text{S}$. Figure 3 shows the drain characteristics for OTFTs of various dielectric materials at fix gate voltage. The drain voltage is changed from 0 to -3V while the gate voltage remains constant at -3V. When a fixed gate voltage is applied, the drain voltage progressively rises, resulting in an increase in drain current that is due to change in dielectric constant in our model. An OTFT with the dielectric HfO_2 has a drain current roughly seven times that of an insulator constructed of SiO_2 . Due to the high dielectric permittivity of HfO_2 , more charges will collect at the DNTT/Dielectric interface. As a response, relative to other dielectrics, dielectric layer of HfO_2 shows

significant increase in transconductance (g_{max}) and current on-off ratio (I_{on}/I_{off}). Figure 4 compares the performance by combining the I_d - V_{ds} curves for various gate dielectrics into a single graph at gate voltage $V_{gs}=-3V$. HfO_2 dielectric has a larger drain current than SiO_2 dielectric. A larger gap between Al_2O_3 and HfO_2 can be seen in both circumstances, which can be attributed to the high-k dielectrics with increased dielectric capacitance.

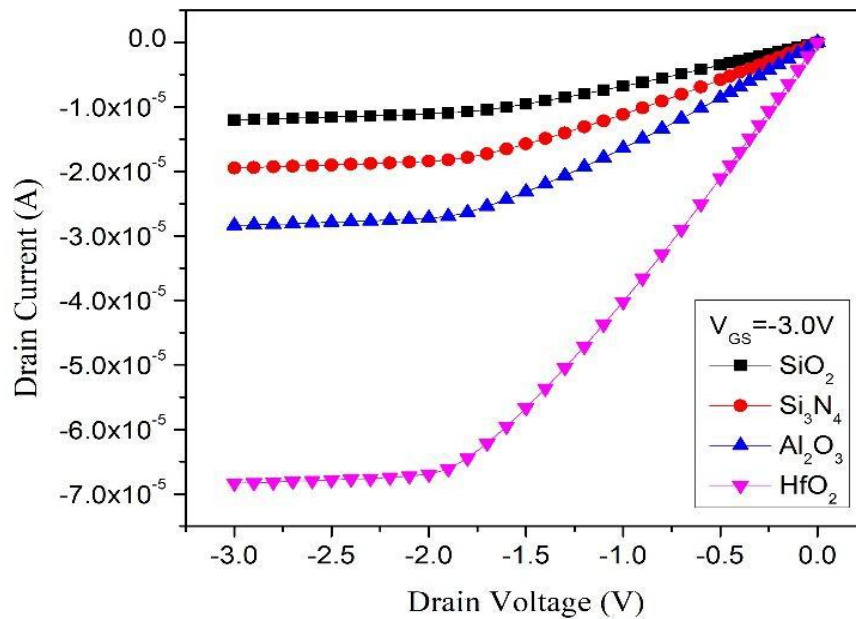


Figure 4. OTFT drain characteristic for different insulators at $V_{gs}=-3V$

Conclusion

Several gate dielectrics are used to design DNTT-based OTFTs, and device properties have been compared. According to simulation data, the gate dielectric has a significant impact on performance of electrical parameters such as threshold voltage (V_{th}), current on-off ratio (I_{on}/I_{off}), transconductance(g_{max}) and maximum drain current(I_{dmax}). HfO_2 dielectric based OTFT has a drain current that is more than seven times that of SiO_2 dielectric. Results suggests that the current on-off ratio (I_{on}/I_{off}) of around 10^9 with HfO_2 dielectric is a good choice for a various memory devices, RFID tags and sensing applications.

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References

1. Baliga, A. K., Kumar, B., & Pandey, Y. (2016). Performance analysis of dual gate OTFT using different gate dielectric materials. 2016 *International Conference on Emerging Trends in Communication Technologies (ETCT)*, IEEE.
2. Deng, L. F., Lai, P. T., Chen, W. B., Xu, J. P., Liu, Y. R., Choi, H. W., & Che, C. M. (2011). Effects of different annealing gases on pentacene OTFT with HfLaO gate dielectric. *IEEE Electron Device Letters*, 32(1), 93–95. doi:10.1109/led.2010.2087314.
3. Sushil Jain, Joshi, Amit. "Label-Free Detection of Biomolecules Using Dielectric-Modulated Top Contact Bi-layer Electrodes Organic Thin Film Transistor."TechRxiv(2022).
4. Deng, L. F., Lai, P. T., Tao, Q. B., Choi, H. W., Xu, J. P., Chen, W. B., Liu, Y. R. (2010). Improved performance of low-voltage pentacene OTFTs by Incorporating La to Hafnium Oxide Gate dielectric. 2010 *IEEE International Conference of Electron Devices and Solid-State Circuits (EDSSC)*. IEEE.
5. Meena, Naresh, and Amit M. Joshi. "New power gated SRAM cell in 90nm CMOS technology with low leakage current and high data stability for sleep mode." In 2014 IEEE International Conference on Computational Intelligence and Computing Research, pp. 1-5. IEEE, 2014.
6. Fan, C.-L., Lin, Y.-Z., Huang, C.-H., Lai, H.-L., & Lin, Y.-Y. (2011). The performance improvement of OTFT by the planar bottom-contact structure with Bi-layer gate dielectric. *The 4th IEEE International NanoElectronics Conference*. IEEE.
7. Guo, X., Xu, Y., Ogier, S., Ng, T. N., Caironi, M., Perinot, A., ... Yan, F. (2017). Current status and opportunities of organic thin-film transistor technologies. *IEEE Transactions on Electron Devices*, 64(5), 1906–1921. doi:10.1109/ted.2017.2677086
8. A.K. Baliga, B. Kumar and Y. Pandey, "Performance analysis of dual gate OTFT using different gate dielectric materials," 2016 *International Conference on Emerging Trends in Communication Technologies (ETCT)*, 2016, pp. 1-4, doi: 10.1109/ETCT.2016.7882961. BN
9. Jain, S., Joshi, A. M., & Bharti, D. (2020). Performance Investigations Of organic thin film transistors on varying thickness of semiconductor material: An experimentally verified simulation study”, *semiconductors*. 54, 1483–1489.
10. Jain, S. K., Joshi, A. M., & Dwivedi, A. D. (2020). Technology and modeling of DNNT organic thin-film transistors. In *Advanced Technologies for Next Generation Integrated Circuits* (pp. 197–211). *Institution of Engineering and Technology*.

11. Meena, N., & Joshi, A. M. (2014). New power gated SRAM cell in 90nm CMOS technology with low leakage current and high data stability for sleep mode. 2014 IEEE *International Conference on Computational Intelligence and Computing Research*. IEEE.
12. Shim, C.-H., Maruoka, F., & Hattori, R. (2010). Structural analysis on organic thin-film transistor with device simulation. *IEEE Transactions on Electron Devices*, 57(1), 195–200. doi:10.1109/ted.2009.2035540
13. Tang, W., Li, J., Zhao, J., Zhang, W., Yan, F., & Guo, X. (2015). High-Performance Solution-Processed Low-Voltage Polymer Thin-Film Transistors With Low K/ high K Bilayer Gate Dielectric. *IEEE Electron Device Letters*, 36(9), 950–952. doi:10.1109/led.2015.2462833
14. ATLAS and ATHENA User's Manual: Process and Device Simulation Software (Silvaco International, Santa Clara (2012).
15. Jain, Sushil Kumar, and Amit M. Joshi. "Dielectric-Modulated Double Gate Bilayer Electrode Organic Thin Film Transistor-based Biosensor for Label-Free Detection: Simulation Study and Sensitivity Analysis." arXiv preprint arXiv:2205.15041 (2022).