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Design of an 8-bit Low Power Flash ADCin 90-nm

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ABSTRACT

This paper presents the 90-nm GPDK CMOS technology library related to eight-bit 487MSps Flash ADC style victimization. As a comparator group and decoder, this design is composed of 2 main blocks. The decoder consists of a 2:1 multiplexer mostly based on one - of - N decoder and Buffer units. As a result, active die space and also the unit of power depletion area were additionally condensed to extend in frequency. The voltage offering capacity varies from ± 1.2V for the system. The simulation results include most of the 0.24 mW power consumption. 204p sec delay, but 0.02LSB and 0.1LSB for the measured DNL and INL.

***Keywords*-Flash, MUX, GPDK, CMOS, DNL, INL.**

I. INTRODUCTION

Analog-to-digital converters are the foremost necessary core units to convert analog info to corresponding digital forms. Which means they will be thought of on bridges between globe and digital world. ADCs are ordinarily utilized in portable devices, transmitter and receiver circuits.Flash ADC is thought because the quickest kind of ADC designers. Foremost necessary role particularly for magnetic browse channel applications, optical knowledge recording, data communication systems requiring high processing rate [5 - 8].

In Figure 1, the completely parallel ADC design is illustrated. Comparison processes with all quantization levels during this design correspond to a rapid analog input voltage level at the same time during only one cycle of the sampling clock signal, while the second part is for changing and obtaining binary data output. This design makes ADC flash because one of all others is the fastest one. Vie by analog blocks is the most active role for the ADC show. These block presentations, particularly comparators used in these flash styles, largely outline the look restrictions associated with translation speed.

Low resolution and better power consumption are the dual famous disadvantages for flash ADCs area units due to higher chip space when placed next to alternative forms of ADC designs. Finally, in the 90nm CMOS technology mistreatment VLSI style platform, a fast and highly lined eight-bit flash ADC style operation is achieved.

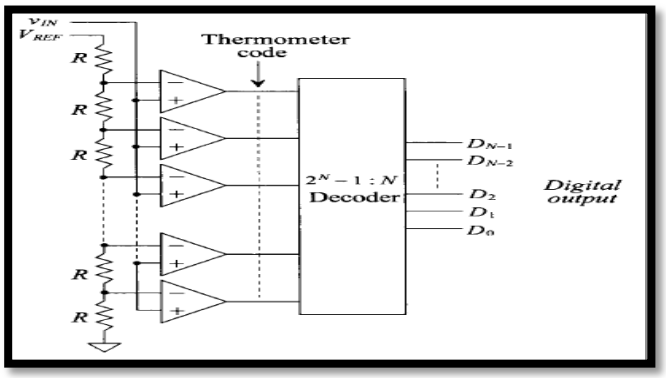

Fig 1: Flash ADC architecture.

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II. 8-BIT FLASH ADC DESIGN

In Figure 2, the configuration of the proposed flash ADC is shown. It comprises an array of comparators and a decoder. The decoder includes a one-of-N decoder and buffer block centered on a 2:1 multiplexer.

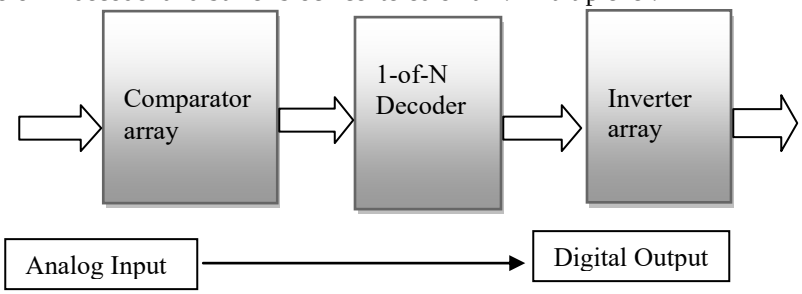

Fig 2: The planned Flash ADC Design

A. Comparator array

The comparator schematic shown in Figure 3 is selected in the built ADC method. Figure 3 and Table I display the junction transistor side ratios, significant DC bias voltages used in the comparator circuit, separately. Money supply and M3 area unit NMOS input differential combine during this circuit, powered by the tail current junction transistor M4.The differential combine is loaded by the feedback loop working diode-connected PMOS transistors (M5 - M6) and cross-coupled PMOS transistors (M0 - M1). The goal of this electrical circuit is to spice up and balance the output resistance of the differential voltage gain obtained by money supply-M3.A new mirror is typed by M9 and M10, and M5 and M7 together provide its reference current. Booting amplified by a standard supply PMOS electronic equipment (M8) is the initial stage output of the comparator. A simple CMOS electrical converter circuit may be the final stage of the comparator (M11-M12).

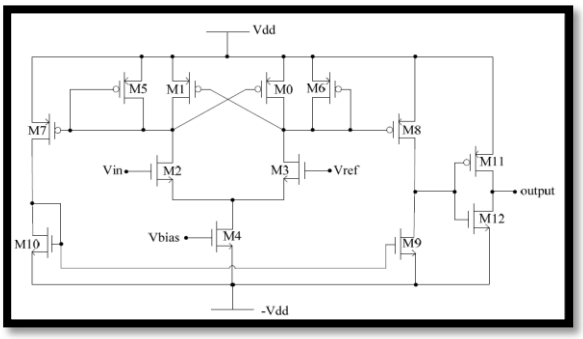

Fig 3: Comparator circuit

B. The 2:1 TG based Mux.

A transmission gate (TG)-based multiplexer circuit used in the decoder is illustrated in Figure 4. There are 2:1 MUXs used in the decoder.

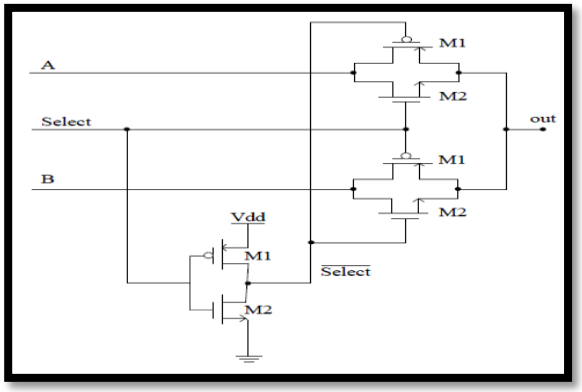

Fig 4: The 2:1 MUX Schematic

C. Buffer

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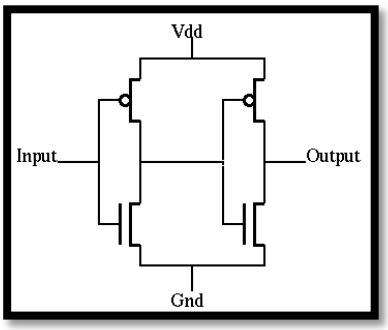

Fig 5: Buffer

This means the schematic of the junction transistor level of a basic two stage buffer. A buffer is used during a digital circuit to postpone a brief amount of a symptom or to intensify a symptom that has worsened to some degree wherever it becomes unintelligible.

D. Resistor Series

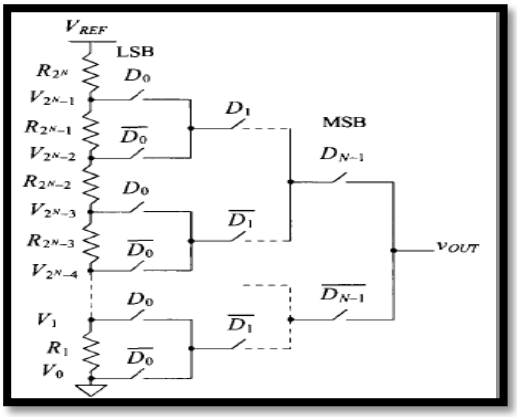

Fig 6: Resistor series circuit.

The resistor series of 2^N is analogous to resistors and controls, and the analog output is simply the resistor voltage split at the selected tap. The V_{REF} is broken down into values of 2^N, each of which is fed into a comparator. The V_1 is compared with each reference value and results in the performance of the comparators in a thermometer code.

III. THE MULTIPLEXER-BASED DECODER.

This section will initially describe the notion behind the primarily dependent decoder granted to the electronic device and secondly describe it, but it is mostly generalized. The primary vital bit of the binary output is high for N-bit flash ADC if the outputs within the measuring device scale area unit logic one are over 1/2.MSB is also the same because of the performance of the measurement device at level 2^N-1. The first measurement system scale is divided into 2 partial measurement system scales, separated by the output at level 2^N-1, to find the value of the second most significant bit (MSB-1).

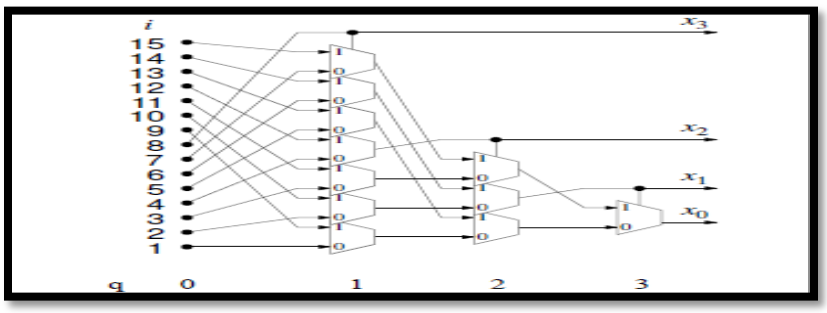

Fig5: N- bit Mux Based Decoder

IV. 8-BIT PLANNED FLASH ADC.

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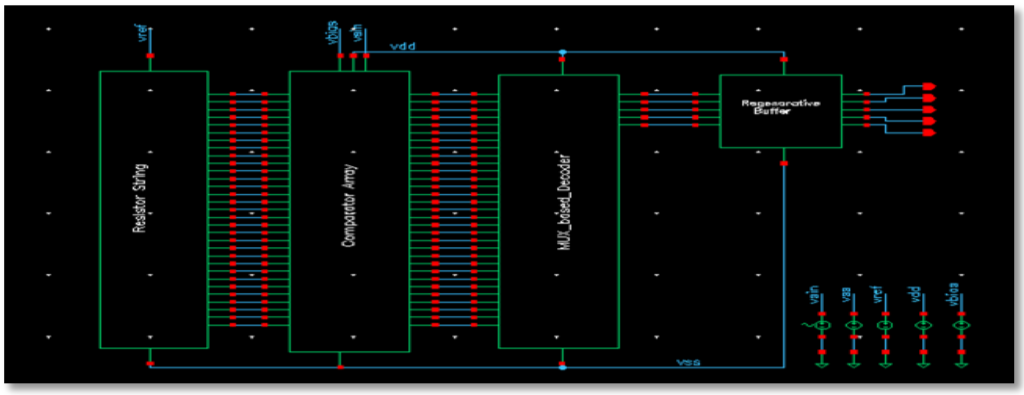
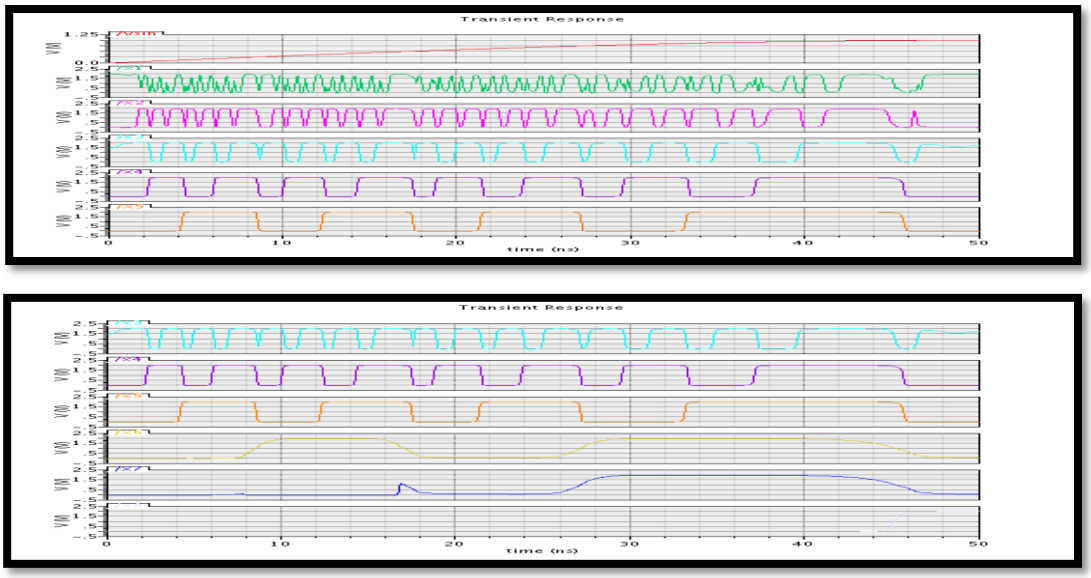


Fig8: Complete schematic of 8-bit Flash ADC using MUX-based Decoder with Buffer.

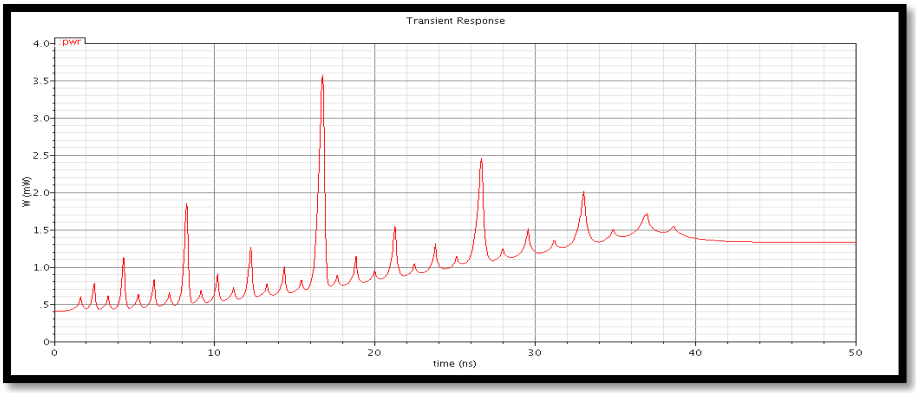
V. EXPERIMENTAL RESULTS.

A. Transient Response.



Graph 1: Simulation result of 8-bit flash ADC

B. Power Consumption.



Graph 2: Power Consumption graph

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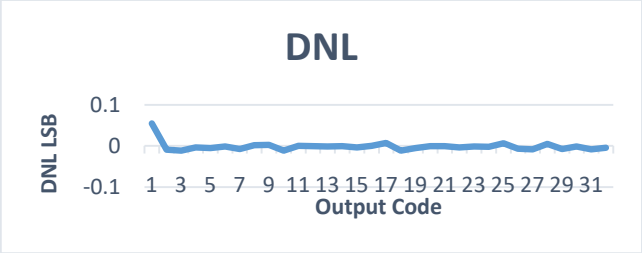
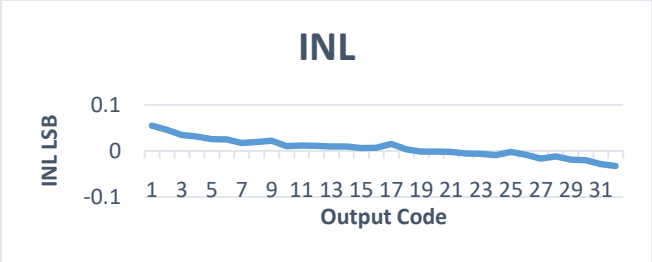
C. Integral non linearity and Differential non linearity

DNL= (input step width -- ideal step width)

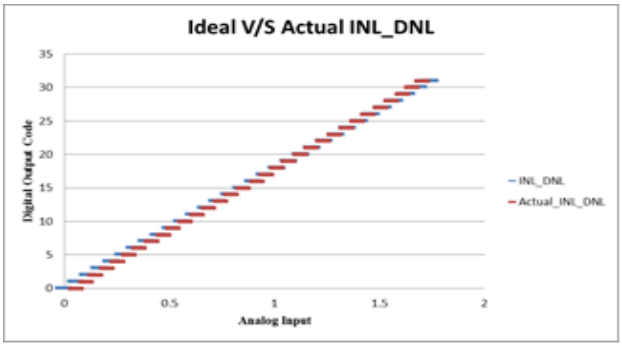
INL= (input voltage -- ideal voltage)



Graph 3:DNL



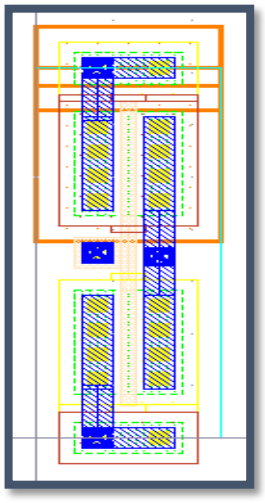
Graph 4:INL



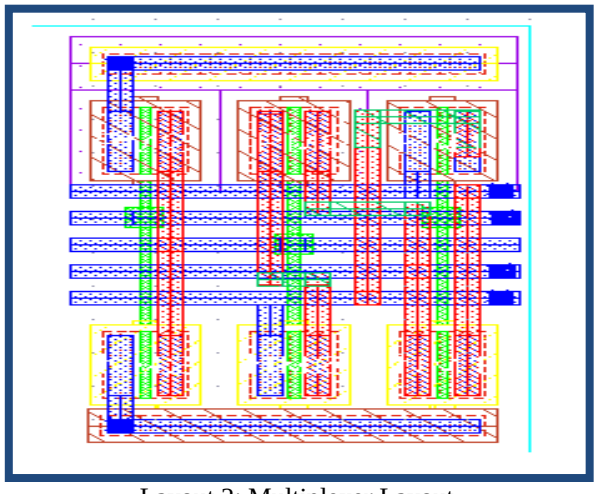
Graph 5: ideal v/s actual INL_DNL

VI. LAYOUT

Timing is incredibly vital, therefore routing for the comparator and electronic device ought to be same, comparator is Associate in nursinganalogy block, and commoncentre of mass is employed for matching input transistors and bury digitization for current mirrors. Electronic device and invertor may be a digital block, therefore there's not a lot of constraints for it. All resistors area unit created into snakelike structure to scale back the realm. High level routing is troublesome, therefore metal four is employed



Layout 1: Buffer layout



Layout 2: Multiplexer Layout

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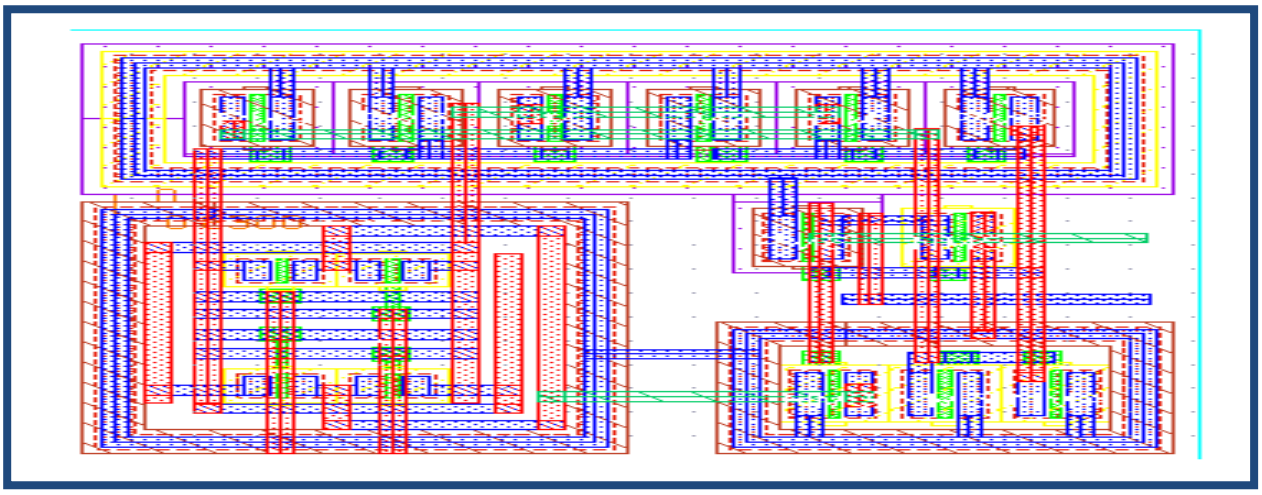
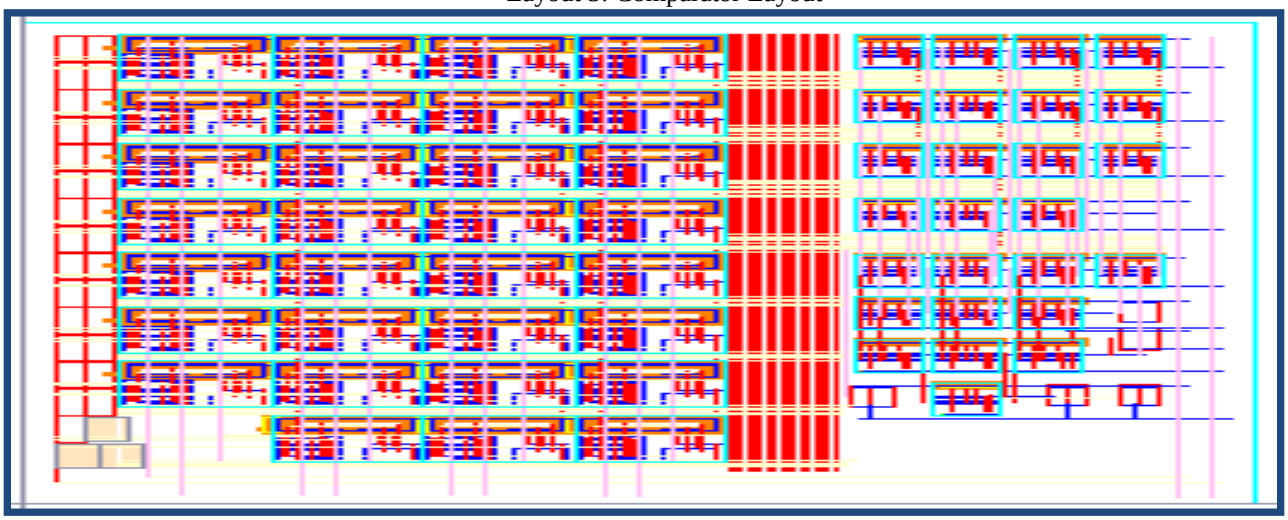


Layout 3: Comparator Layout



Layout 4: Flash ADC

Table 3: Comparison of the performance

	Present work	**[2]**	**[3]**	**[5]**	**[6]**
Type	Flash	Flash	Flash	Flash	Flash
Bit-size	8bit	6	8	8	8
Input voltage	1.2v	1.8v	1.8v	2.5v	1.2v
GPDK	90nm	90nm	90nm	90nm	90nm
Power Consumption	0.24mW	70mW	78mW	120mW	1.3mw
Delay	205 Pico Sec	-	-	-	0.08ns
Differential non linearity	0.032LSB	0.35	0.16	0.8	-
Integral non linearity	7.44LSB	0.25	0.21	1.4	-
Speed	5.87GS/S	4Gs/s	5Gs/s	800Ms/s	6Gs/s
Signal to Noise Ratio	33.86db	-	-	40.1db	-
Input frequency	40GHZ	-	100Mhz	10Mhz	100MHZ
Total space	0.03 micro m^2	0.9mm^2	0.88mm^2	0.32mm^2	--

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VII. CONCLUSION

In conclusion, an eight - bit 487MSps full-flash ADC was with success designed in 45nm CMOS technology. Consistent with the simulation results, the projected ADC is very linear with the worst case DNL of 0.02LSB and INL of 0.1LSB, and additionally has low power consumption worth 1mW.

The performance outline Table 2. Supported the simulation results, the two x one MUX-based decoder structures improve the performance in terms of speed and power consumption. Moreover, it's additionally believed that, the projected ADC design is enticing for sty leers from design complexness purpose of read. The layout photograph of the entire convertor is shown in V. Layout Section. Comparison result shown in Table three and Table four.

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